Modeling and Simulation of HEMT GaN Power devices under Electrothermal stresses

Dissertation submitted to
Visvesvaraya National Institute of Technology, Nagpur
In partial fulfillment of the requirements for the award of the degree

Master of Technology
in
VLSI Design

by

Akash Kumar Dixit
(MT23MVD012)

Under the guidance of

Dr. R.B. Deshmukh, Dr. N.D. Gupta

Dr. Beydoun Bilal

Centre for VLSI and Nanotechnology
Visvesvaraya National Institute of Technology
Nagpur 440010 (India)

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Visvesvaraya National Institute of Technology, Nagpur

DECLARATION

I, **Akash Kuma Dixit**, hereby declare that this dissertation titled **"Modeling and Simulation of HEMT GaN Power devices under Electrothermal stresses"** is carried out by me in the **Center for VLSI and Nanotechnology** of Visvesvaraya National Institute of Technology, Nagpur. The work is original and has not been submitted earlier whole or in part for the award of any degree/diploma at this or any other Institution / University.

Akash Kumar Dixit
Date:

CERTIFICATE

This is to certify that the dissertation titled **"Modeling and Simulation of HEMT GaN Power devices under Electrothermal stresses"** is submitted by **Akash Kumar Dixit (MT23MVD012)** in partial fulfillment of the requirements for the award of **Master of Technology in VLSI Design,** VNIT Nagpur. The work is comprehensive, complete and fit for final evaluation.

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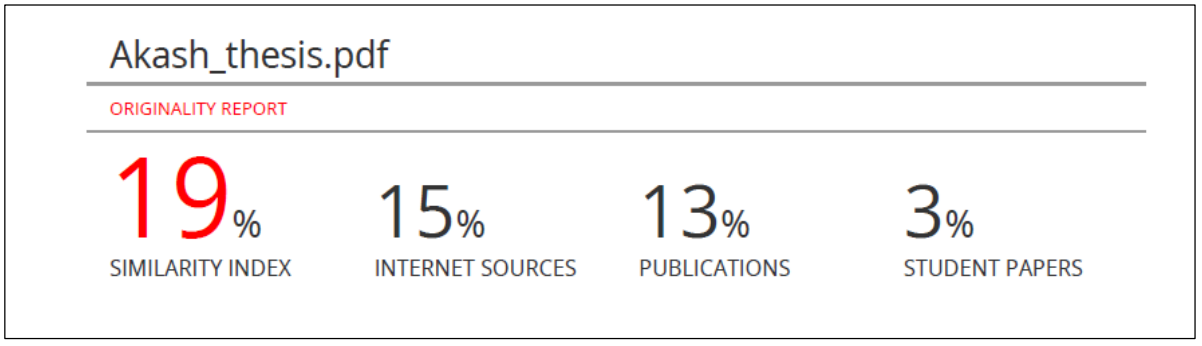

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Acknowledgement

First and foremost, I would like to thank all my supervisors, **Prof. R.B. Deshmukh(VNIT), Dr. Nikhil Deep Gupta(VNIT),** and **Dr. Beydoun Bilal (CESI)** for their support and guidance throughout the course. I am grateful for their encouragement, which gave me the motivation I needed to conduct my research. I have learned a lot.

I would like to express my sincere regards for the Institute Director, **Prof. P. L. Patel, Dean (Acad.) Prof. V.R. Kalamka** and **Associate Dean (Acad -PG/PhD) Prof. R. V. Taiwade** for their unwavering support for student academic requirements.

I would like to express my sincere gratitude to Head of Department, **Prof. S. B. Dhok, Prof. R. M. Patrikar, Dr. G.C Patil** and **Dr. Vasu Pulijala** of the department who provided me with all the assistance I needed to dig deeper into the subject and comprehend the field. I owe them for their insightful advice, creative suggestions, critical analysis of the work, and most importantly their support of my research throughout the course.

I've had a lot of friends who have kept me sane during these trying years. Their concern and support enabled me to overcome obstacles and maintain my concentration on my graduate studies. I cherish our friendship and am incredibly grateful for their support.

Finally, I would like to thank my family members for their constant support and encouragement, and last but not the least I am very thankful to Life, who provides me good health and good people around me.

Akash Kumar Dixit

Abstract

Gallium nitride (GaN) has become a crucial component in high-power and high-frequency electronics because of its large and direct bandgap, high breakdown electric field, and fast electron saturation velocity. Specifically, through spontaneous and piezoelectric polarization effects, the AlGaN/GaN heterostructure makes it possible for a high-density two-dimensional electron gas (2DEG) to emerge at the interface, improving device performance and carrier mobility. Because of its intrinsic safety and compatibility with traditional gate drivers, normally-off p-GaN gate HEMTs have become more popular among the several GaN-based transistor topologies for power switching applications.However, electrothermal strains, particularly when operating at high voltages or temperatures, frequently limit the performance of these devices by creating trap states within crucial device layers. These traps have the potential to reduce current levels, increase gate leakage, and jeopardize device reliability, especially in the buffer zone and beneath the gate.

The impact of electrothermal stress-induced trap formation in p-GaN HEMTs was examined in this work using Sentaurus TCAD simulations. Experimental DC and AC data were used to model and calibrate device architectures. The modeling of trap-assisted tunneling (TAT) and deep-level trap behavior due to high electric fields and localized heating was of special interest. The sensitivity of Id–Vd and Id–Vg features to trap profiles in the barrier and buffer layers, as well as their transient behavior, were investigated using simulations. Analysis was also done on how trap spatial distribution and energy level relate to gate leakage and current collapse. Field plates were not used in the simulated structures to isolate and emphasize the impacts of intrinsic trap generation mechanisms, in contrast to several methods in the literature. In addition to offering insight into design considerations for enhancing reliability in p-GaN gate HEMTs for high-power applications, the results highlight the crucial role that electrothermal-induced trapping plays in performance degradation.

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Abbreviations

GaN	Gallium Nitride
AlGaN	Aluminium Gallium Nitride
CB	Conduction Band
CTE	Coefficient
VB	Valence Band
EF	Electric Field
BV	Breakdown Voltage
2DEG	2 Dimentional Electron Gas
CVD	Chemical Vapor Deposition
HEMT	High Electron Mobility Transistor
FET	Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOCVD	Metal-Organic Chemical Vapor Deposition

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1

INTRODUCTION

1.1 Background

When the transistor was created in the United States at the end of 1947, the development of semiconductor technology really got underway. John Bardeen, Walter Brattain, and William Shockley, who later won the Nobel Prize in Physics in 1956, conducted extensive research at Bell Laboratories that resulted in this groundbreaking discovery. This invention's origins can be found in the years leading up to World War II, when researchers started examining the characteristics of silicon and discovered the two basic varieties of semi-conductors, N type and P type. The basis for these divisions was the type of impurities, sometimes referred to as dopants, that were added to the silicon crystal lattice. It soon became clear that these findings would have a significant impact on the electronics industry.

The transistor has significantly changed modern living since it was created. It is the foundation of modern electronic systems, together with its successor, the MOSFET. These parts are essential to many different industries, such as telecommunications, which have fueled the explosive growth of the global electronics market in recent decades; power electronics, which gained momentum with the expansion of railway systems and electric motors; and microelectronics, which sparked the development of computers.

Since 1947, there has been constant progress in the field of electronics, both in terms of design and fabrication techniques as well as materials. Because of its abundance and well-understood characteristics, silicon is still the most extensively used material in semiconductor technology. However, researchers have shifted their attention to compound semiconductors for advanced and optoelectronic applications. These materials include group IV semiconductors (SiC and SiGe), III-V group compounds (GaAs and GaN), and II-VI group compounds (CdTe and ZnSe).

Scientists have produced ternary semiconductors, such as AlGaN, GaInAs, and AlGaAs, by mixing binary molecules, providing even more design flexibility. When compared to silicon, these more recent materials have better electrical properties. For instance, the electron mobility of gallium arsenide (GaAs) is six times greater than that of silicon, and the critical electric field strength of gallium nitride (GaN) is around 10 times more.

In 1968, Maruska and Tietjen developed the Hydride Vapor Phase Epitaxy (HVPE) technique to grow GaN on sapphire substrates, which marked the beginning of the production of high-quality GaN films. Sapphire was chosen due to its affordability in comparison to other substrates, such as silicon carbide (SiC), and its chemical inertness, particularly in conditions that are rich in ammonia. However, the majority of early GaN films were polycrystalline, which limited their applicability in the manufacturing of devices.

Maruska's 1969 discovery that GaN growth, not degradation, could take place in an ammonia atmosphere at temperatures higher than 600°C was a significant breakthrough. He produced the first single-crystalline GaN film by raising the growing temperature to 850°C, which is comparable to the temperature used for GaAs. Nevertheless, these films showed extremely high levels of inadvertent n-type doping, which is frequently ascribed to nitrogen vacancies. Given that oxygen can function as a shallow donor when nitrogen atoms are substituted, subsequent research suggested that oxygen impurities are the most likely cause of this behavior. Finding an appropriate p-type dopant was a major obstacle. Based on its success doping GaAs and GaP, zinc (Zn) showed some promise, but it made GaN films insulating without allowing for full p-type conductivity. Maruska didn't propose magnesium (Mg) as a more practical p-type dopant until 1972.

Setbacks and the Breakthrough in P-type GaN

Despite initial hope, ongoing challenges caused GaN development to significantly slow down in the late 1970s. Progress was hampered by problems like inappropriate substrate materials, unpredictable n-type conductivity, and the inability to create conductive p-type films. By 1982, worldwide GaN research had all but stopped, with very few publications appearing.

Isamu Akasaki's successful production of conductive p-type GaN films in 1989 marked a turning point in the field. During cathodoluminescence (CL) experiments employing scanning electron microscopy (SEM), this discovery was made. This behavior was described by Van Vechten and associates in 1992, who attributed it to the creation of Mg-H complexes in the GaN matrix. The acceptor behavior of magnesium was passivated

by these compounds. These complexes were broken apart by the electron beam's energy, which released the magnesium acceptors and activated the p-type conductivity.

Towards Modern GaN Technology: MOCVD and Device Integration

When Amano et al. suggested employing an AlN nucleation layer in MOCVD to improve the quality of GaN films in 1986, it was another noteworthy advancement. This buffer layer, which was produced at roughly 600°C, enhanced the generated films' structure and electrical properties by correcting the lattice mismatch between sapphire and GaN. The primary technique for producing high-quality GaN layers for electrical and optical applications is currently MOCVD.

GaN research saw a rebirth in the 1990s, with quick advancements resulting in commercial feasibility. HEMTs were made possible by Khan et al.'s 1991 demonstration of 2DEG production at AlGaN/GaN heterojunctions. The first GaN-based MESFET and HFET devices were subsequently created in 1993 and 1994, respectively. Furthermore, by creating the first continuous-wave blue GaN laser diodes (LDs) in 1996 and high-brightness blue GaN LEDs in 1993, Shuji Nakamura and associates accomplished noteworthy advancements in the field of optoelectronics.

Why Normally off Device

In contemporary power electronics, the development of normally-off (E-mode) GaN HEMTs is crucial for ensuring safety, simplifying circuit design, and enhancing compatibility with existing control systems. Traditional AlGaN/GaN HEMTs are inherently normally-on due to the formation of a 2DEG at the heterojunction interface, a result of strong polarization effects, even when the gate bias is not there. This default conductive state poses safety concerns, particularly in high-voltage applications, as it necessitates additional fail-safe mechanisms to prevent unintended current flow. Conversely, normally-off HEMTs remain non-conductive at zero gate bias, turning on only when a positive voltage is applied, thereby offering a fail-safe operation that is highly desirable in power systems .

Several engineering strategies have been explored to achieve normally-off behavior in GaN HEMTs. These include gate recessing, fluorine ion implantation, and the incorporation of a p-type GaN (p-GaN) gate layer. Among these, the p-GaN gate approach

has gained significant traction due to its effectiveness and scalability. In this configuration, a p-type GaN layer is introduced atop the AlGaN barrier, forming a p-n junction that depletes the 2DEG under zero gate bias, thus achieving the desired normally-off characteristic .

The implementation of p-GaN gate HEMTs has demonstrated promising results, with devices exhibiting threshold voltages exceeding +1 V, low off-state leakage currents, and robust on-state performance. For instance, state-of-the-art p-GaN gate transistors with 600 V breakdown strength have shown threshold voltages around +1 V, off-state leakage currents of 10 nA/mm at zero gate bias, and drain currents of 0.4 A/mm under typical operating conditions . These attributes make p-GaN gate HEMTs suitable for high-efficiency power conversion applications, including those in consumer electronics, automotive systems, and industrial equipment.

Despite these advancements, challenges such as gate leakage currents under high forward bias and reliability concerns related to the metal/p-GaN interface persist. Ongoing research focuses on optimizing the p-GaN layer's doping concentration, improving gate metal selection, and refining fabrication processes to enhance device performance and reliability . As these issues are addressed, normally-off GaN HEMTs are poised to play a pivotal role in the next generation of power electronic systems.

Present and Future of GaN Based Electronics

GaN is now a top material for both research and commercial applications as a result of these developments. GaN HEMTs are currently on the verge of becoming widely used in microwave and high-power electronics, while GaN based LEDs and laser diodes have already found success in the mass market. However, persistent issues with device dependability, material quality, and process scalability still necessitate targeted investigation. For GaN devices to be integrated into reliable, high-performance systems over the long term, their full potential must be realized, especially when exposed to electrothermal stress.

Motivation

32% of GaN HEMT failures in aerospace applications are linked to trap-assisted thermal runaway. Industry-reported *R*on degradation >40% under 100 V stress

1.3 Thesis Organisation

The five chapters that follow are covered in this thesis.

Chapter1:

This chapter has the introduction and the background of the project.

Chapter2:

The most popular wide band gap materials GaN, AlGaN, AlN, and SiC that can be utilized to create HEMTs will be covered in the second chapter. I'll also go over the characteristics that make these materials ideal for high voltage and high frequency applications, as well as LEDs.

Chapter3:

The 2DEG creation at the interface of AlGaN/GaN as well as the impacts of traps, particularly the current collapse process, will be the main topics of this chapter. Since the growth process has not yet been refined, a lot of imperfections are present in the structure, which is why WBG semiconductors, a novel technology, suffer from trapping effects.

Chapter4:

In this chapter, we will focus on the Structural details of the device and what is the significance of every layer.

Chapter5:

My simulation activity is covered in this chapter, beginning with the DC simulations and covering both IdVg and IdVd features. In order to determine whether the existence of traps beneath the gate could be the source of the leakage that severely affects this type of device, I always include some simulation findings in the chapter. This chapter also presents the conclusion and future work.

2

LITERATURE REVIEW

This chapter will describe the application fields of the most prevalent Wide band gap materials, including GaN, AlN, and SiC, as well as their material properties and compare them to those of semiconductors such as Si and GaAs.

The use of WBG materials in optoelectronic and electrical applications has garnered a lot of interest in the past ten years. The many material qualities in relation to silicon, the most common material in electronics, are the causes of this interest. Usually produced with a wurtzite structure, III-V compound semiconductors have a bandgap between 1.0 eV and 6.0 eV. Short-wavelength LEDs and high power electronics fields requiring high breakdown voltage and resilience to high temperatures benefit from this extremely wide band gap. Because of its high inherent electron concentration, or 2DEG, which allows for fast carrier transport, these materials are also utilized in radio high applications.

2.1 Materials properties

Wide bandgap (Eg) semiconductors have a high critical electric field (Ec), which enables them to operate effectively at high temperatures and in high-voltage applications. Wide bandgap materials like SiC and GaN have a breakdown field strength that is nearly ten times larger than that of conventional semiconductors like Si, GaAs, and InP, as Table 2.1 illustrates.

Furthermore, the intrinsic carrier concentration is impacted by the wide bandgap. Intrinsic carriers, which are influenced by temperature, might impair the functionality of electronic devices that use regulated current modulation. Excessive leakage currents render the material unsuitable for electronic applications if the inherent carrier density approaches 10^{15} cm^3.

Wide bandgap semiconductors are becoming more popular for high-temperature applications because of this. Performance degradation is avoided by their wider bandgap, which guarantees that intrinsic carrier concentrations remain low even at very high temperatures.

Property	GaN	AlN	InN	SiC	Si	GaAs
Band Gap (Eg)[eV]	3.44	6.2	1	3.26	1.12	1.43
Electric breakdown field (Ec) [MV/cm]	3.0	1.4 - 1.8	3.0	0.3	0.4	0.5
Saturated electron velocity (*vsat*)[x $10^7 cm/s$]	2.5	1.7	4.5	2.0	1.0	1.0
Electron mobility (μn) [$cm^2/V \cdot s$]	900(bulk) 2000(2DEG)	135	3200	700	1500	8500
Electron effective mass (*mc*) [*m*0]	0.22	0.4	0.11	0.2	1.18	0.63
Hole effective mass (*mv*) [*m*0]	0.8	3.53	0.27	1.0	0.55	0.52
Lattice constant [$^{\circ}A$]	3.175	3.111	3.533	3.073	5.431	5.653

Table 2.1: Material Properties

2.1.1 Gallium Nitride

The fundamental component of the III-N group of compounds is gallium nitride. It is usually employed in domains that demand high breakdown voltage and quick carrier transmission. GaN is utilized in a variety of FET and HEMT devices as a channel material. The comparatively low electron mobilities (μn), which are 900 cm^2/V s for GaN and roughly 700 cm^2/V s for SiC, are a major drawback of creating transistors from bulk GaN and SiC. In contrast, GaAs has an extremely high electron mobility (8500 cm^2/V s), which is why field-effect transistors are frequently made using GaAs.

WBG semiconductors typically have very high saturation velocity values, which are attained at high electric fields, but minimal mobility. In fact, interface qualities, rather than inherent material transport properties, are primarily responsible for the enormous success of III-N materials. The interface permits the creation of an n-channel, known as two-dimensional electron gas (2DEG), at the $Al_xGa_{1-x}N$/GaN interface in the case of the III-N

heterostructure. Without additional impurity doping, this electron gas naturally produces incredibly high carrier concentrations.

For applications requiring high-frequency, high-power devices, the heterojunction's 2DEG's mobility and saturation velocity are ideal. In contrast to bulk GaN and SiC, the room temperature mobility of the 2DEG, which is normally between 1200 cm^2/Vs and 2000 cm^2/Vs is noticeably better. Because of piezoelectric and spontaneous polarization-induced effects, the AlGaN/GaN structure has high 2DEG sheet charge density (ns) (experimental values (10^{13} cm^2)). Comparing the measured sheet charge density to the $Al_xGa_{1-x}As/In_xGa_{1-x}As$ and $In_xAl_{1-x}As/In_xGa_{1-x}As$, the former is roughly ten times better.

Property	GaN	AlN	InN	SiC	Si	GaAs
Thermal conductivity (κ) [$W/cm \cdot K$]	1.3-2.1	2.85	0.45	3.7-4.5	1.5	0.5
Relative permittivity (ϵr)	9.0	9.14	15.3	10.1	11.8	12.8

Table 2.2 : III-N and other materials relative permittivity and thermal conductivity (at 300K)$Al_xGa_{1-x}N$

Semiconductor material's thermal conductivity (κ) (Table. 2.2) is a crucial characteristic since it indicates how easily dissipated power can be removed from the device. At high temperatures, devices with poor thermal conductivity perform worse. Conventional semiconductors, especially GaAs and InP, are generally poor thermal conductors. On the other hand, SiC is a great thermal conductor and a strong option for GaN development. GaN can be grown on SiC without causing many flaws since, aside from thermal conductivity, these two materials have fairly similar lattice constants.

A transistor's capacitive loading is indicated by its relative permittivity (εr) (table. 2.2), which also influences the device terminal impedances. The permittivity values for WBG semiconductors are significantly lower than those for conventional semiconductors, as the table below demonstrates. For a given impedance, this enables a GaN device, for instance, to have an area that is roughly 20% larger. Consequently, the creation of more currents and microwave output power is made possible by this expanded region.

Several disadvantages exist for high-power/high-frequency applications. Low heat conductivity and high substrate costs are two of them. In high-power applications, the latter makes efficient heat removal more challenging. Therefore, having high-quality materials is essential for more reasons than just these, as it helps prevent ruptures that may result from structural flaws.

Property	GaN	AlN	InN	SiC	Si
$\alpha\ [10^6\ K^{-1}]$	3.1	2.9	3.2	2.6	4.3

Table 2.3 : Comparing the Thermal Expansion Coefficient of different Semiconductors (at 300K)

The property shown in Table 2.3 CTE is crucial for growth. GaN and AlN will work well on SiC because of their similar values, as can be seen. There is a noticeable difference between sapphire and silicon, and the material produced will be of lower grade.

2.1.2 Aluminium Nitride (*AlN*)

Aluminum nitride (AlN) is a ultra-wide bandgap (UWBG) semiconductor with exceptional properties for next-generation electronic and optoelectronic applications. With a direct bandgap of 6.42 eV at room temperature

As shown in table 2.3, AlN has an intrinsic thermal conductivity that is superior to all other semiconductors, with the exception of BN, SiC, and diamond, and its thermal expansion is comparable to that of GaN.[5] Another purpose of the AlN nucleation layer is to restrict the GaN buffer layer's breakdown voltage (BV). It was demonstrated that the thickness of the AlN nucleation layer had a significant impact on the produced devices' BVs. AlN is a potentially appealing substrate material because of these properties.

This material's high band gap enables the band gap of AlGaN to be altered in a wide range from the GaN value to the AlN value. The band gap range of InAlN material can be much larger when InN is used in place of GaN. Monte Carlo (MC) simulations are done to study the electron transport in wurtzite AlN. The comparatively high effective electron mass (mc) of 0.48 and the wide band gap are the electrical features. These parameters

result in a saturation velocity of $1.4 \times 10^{17} cm^2$ an extremely high field of 450kV cm^2, and a low field mobility of $135 cm^2 V^{-1} s^{-1}$ at room temperature.

2.1.3 Aluminium Gallium Nitride ($Al_xGa_{1-x}N$)

For AlGaN a law name vegards law is being used to find out the properties of this very impotant ternary compound GaN(P_{BN}) and AlN (P_{AN}):

$$P_{AxB1-xN} = x \cdot P_{AN} + (1 - x) \cdot P_{BN} \quad (2.1)$$

It can so gather data on the lattice constant, dielectric constant, energy gap, and other crucial electronics parameters. The band gap and other physical properties can be adjusted from the GaN to the AlN ones as needed by changing the aluminium fraction (x). This enables, for instance, the creation of more effective barriers for high power applicationand optoelectronic applications.

2.2 Substrate Material

The selection of substrate material is influenced by a range of critical factors aimed at ensuring optimal performance and manufacturability. Key considerations include the substrate's thermal conductivity and its coefficient of thermal expansion, which are essential for thermal management and compatibility with other materials. Electrical insulation capability is also a major factor, as is the overall cost-effectiveness, including the price per unit area. The substrate's availability in the desired diameters plays a role in manufacturing scalability. Additionally, high crystal quality with minimal residual defects is sought to maintain device reliability. Surface characteristics and defect densities further impact device performance. Mechanical and chemical stability, especially concerning processes like wafer thinning and via-hole etching, are equally important. Lastly, parameters such as wafer warp and bowing are evaluated to ensure structural integrity and ease of processing during fabrication.

The most popular substrates that are appropriate for GaN growth, apphire, Silicon Carbide, and Silicon, will be discussed in this section.

2.2.2 Sapphire Substrates

Sapphire (Al_2O_3) is the most common substrate for GaN epitaxial growth, prized for its semi-insulating properties, thermal resilience (withstanding temperatures >1,000°C), and affordability (~$100 per 2-inch wafer). However, its applicability in high-power electronics is limited by a thermal conductivity of just 0.47 W/cm·K, which restricts heat dissipation, and significant crystalline mismatches 13% lattice disparity and 34% thermal expansion difference compared to GaN. These mismatches induce threading dislocations (>10^8 cm^{-2}) and wafer bowing during cooling, necessitating complex buffer layers to mitigate strain. Despite these challenges, sapphire remains viable for optoelectronics and low-power RF devices where cost outweighs performance constraints.

2.2.2 Silicon Carbide Substrates

Silicon carbide (SiC) offers superior performance for high-frequency GaN devices due to its exceptional thermal conductivity (3.7–4.5 W/cm·K), which is nearly tenfold higher than sapphire, and closer crystalline alignment with GaN (3.4% lattice mismatch). This compatibility reduces dislocation densities to ~10^7 cm^{-2} and minimizes thermal stress (25% expansion mismatch), enabling robust high-power operation. Commercially available in 4–6 inch diameters with resistivities exceeding 10^9 Ω·cm, SiC-based GaN HEMTs achieve power densities of 12 W/mm in X-band (8–12 GHz) and over 30 W/mm in C-band (4–8 GHz) using advanced field-plate designs. While its high cost ($500–800 per 4-inch wafer) limits mainstream adoption, SiC is indispensable for aerospace, defense, and emerging 5G infrastructure, where thermal and electrical performance are critical.

2.2.3 Silicon

[2] Silicon (Si) offers several advantages as a substrate for GaN heteroepitaxy, such as low production costs, wide availability, moderate thermal conductivity (~1.5 W/cm·K at 300 K), and compatibility with existing silicon-based electronics. However, its use is challenged by a substantial lattice mismatch (~17%) and a very high thermal expansion coefficient mismatch (~56%) relative to GaN. Furthermore, Si substrates typically exhibit lower electrical isolation (10–30 K·cm), which can lead to greater power losses in high-frequency applications.

Despite these limitations and the unique epitaxial growth challenges associated with GaN on Si distinct from processes used on sapphire or semi-insulating SiC—recent

advancements have demonstrated that comparable device performance can still be achieved. Through the development of specialized epitaxial techniques tailored for Si, researchers have successfully produced high-performance GaN devices on this cost-effective platform.

2.3 Applications

GaN and related alloys have a straight bandgap, which makes them suitable for both optical and electrical applications. GaN's bandgap is 3.44 eV at 300 K, which is equivalent to a wavelength in the optical spectrum's near ultraviolet region. Figure 2.2 presents a graph illustrating the relationship between bandgap energy and lattice constant, overlaid with the visible optical spectrum.

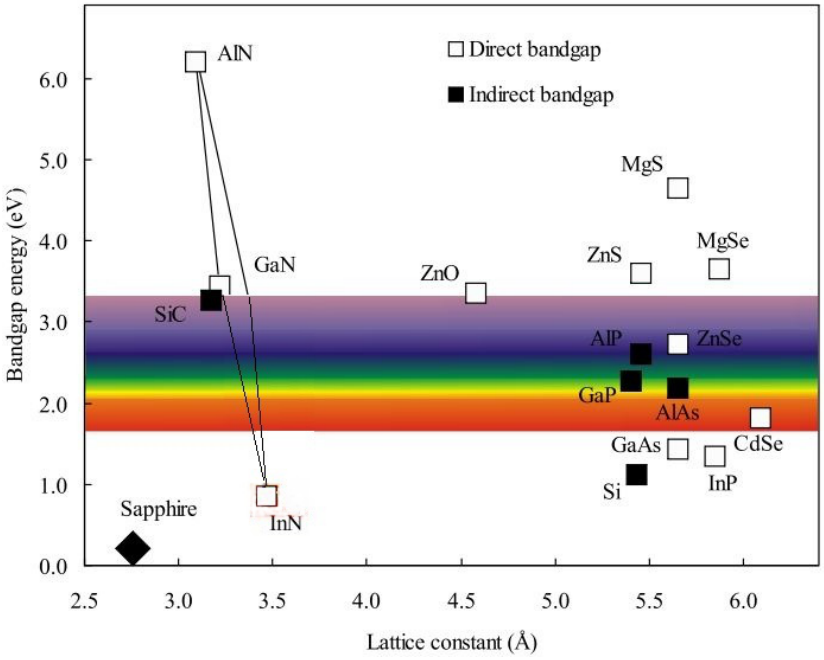


Figure 2.2: Relationship between bandgap energy and lattice constant

As can be observed, the $Al_xIn_yGa_{1-x-y}N$ alloys span band gap energies between 1 eV and 6 eV, which correlate to deep UV to red wavelengths.

2.3.1 Optical Applications

Optical applications like LEDs and lasers, which have recently gained a lot of popularity due to advances in their efficiency and dependability as well as a decline in

their cost. These factors contributed to the rapid growth of the LED and laser markets in recent years. In fact [6], Strategies Unlimited estimates that the LED market, which peaked in 2006, is poised to break out of its current period of slow growth. By 2011, emerging applications including lighting will propel the industry to $9 billion. [7] Strategies Unlimited, a US-based market analyst, projects a 9% yearly growth rate for lasers.

2.3.2 LED

Low power consumption, great efficiency, and long lifespan are the primary financial advantages of LED-based lighting. Furthermore, LEDs' solid-state construction makes them resistant to vibration, frequent switching.

Additional significant GaN-based LED applications include water purification systems, medical (sensors, surgical goggles), general illumination (interior and exterior), white light (flash lights, automobile headlights, etc.), and back lighting (cell phones, laptops, etc.). Red, green, and blue pixels on the screen can be combined to generate a full-color image.. A bright blue LED was all that was required to make a flat LED-based television set a reality.

These devices were made utilizing II-VI materials like zinc oxide (ZnO) or SiC. SiC LEDs were inefficient, nevertheless, due to their indirect bandgap. The primary drawback of the II-VI compound-based devices was their far too limited lifespan for commercial use. Therefore, the intended display applications could not make advantage of these devices.

2.3.3 LASER

Red AlInGaP-based and infrared AlGaAs-based laser diodes (LDs), like those used in modern CD and DVD players, have been in use for many years. A CD's pit size needs to be reduced in order to enhance its storage capacity. In order to focus on the lower pit size, a shorter wavelength LD is needed. The LD used in the most recent generation of DVD systems has an emission wavelength of 650 nm. The market for DVD systems has grown significantly during the past few years. Most of these devices, however, are read-only and rely on a 5 mW AlInGaP LD emitting at 650 nm.

A recordable DVD was clearly required for future market advancements. Higher output power (usually 30–40 mW) from the 650nm LD was needed for this. Higher power is needed to attain even quicker read/write rates. Optical high-density data storage systems

for PCs and next-generation DVD player-recorders will be built on top of GaN-based blue-violet LDs with an emission wavelength of 405 nm.

2.3.4 Electronics Applications

Strategies Unlimited. GaN's high electric breakdown field and, consequently high electron saturation velocity make it a great choice for high-power/high-temperature microwave applications. One of the two prerequisites for high-power device performance is the application of high supply voltages, which is made possible by the wide bandgap and results in high BV. Furthermore, the material can tolerate high operating temperatures (300 °C to 500 °C) because to its wide bandgap..

2.3.5 Commercial Applications

Gallium nitride (GaN) based technologies are poised to become commercially mainstream. One of the earliest areas of adoption is likely to be in high-efficiency, high-linearity power amplifiers used in base stations for 3G and next-generation wireless broadband networks, particularly in the S-band frequency range (2–4 GHz). Other promising high-volume applications for GaN electronics include high-frequency wireless links, power electronics for hybrid electric vehicles (especially in DC-AC conversion), and various forms of high-temperature and high-voltage electronics such as inverters, plasma display drivers, and sensors (including MEMS and Hall-effect sensors for automotive systems). In contrast, conventional silicon devices such as p-i-n diodes and insulated-gate bipolar transistors (IGBTs) dominate many high-power systems like three-phase motor drives. However, these Si-based components typically operate within limited junction temperature ranges (150–175°C) and often require large cooling systems—like heat sinks or liquid cooling—making integration more complex and costly.

GaN-based power electronics offer major advantages for high-temperature environments. Their ability to function at elevated junction temperatures, up to approximately 600°C with minimal reverse leakage, makes them suitable for use in demanding sectors such as renewable energy, aerospace, and industrial automation. Wide bandgap (WBG) materials like GaN also enable faster switching speeds and better efficiency even at room temperature, positioning GaN as a key enabler for next-generation power devices that outperform silicon across a wide range of conditions.

2.3.6 Military Applications

To demonstrate the high expectations, research programs have concentrated on reaching hero figures for output power densities and current densities at microwave frequencies. Nevertheless, the new programs begin with the fundamentals (material growth, etching, and contacts) and progress through the discrete device stage before arriving at GaN-based MMICs.In order to improve repeatability and reliability, the emphasis currently is on comprehending the physical causes of device failures and creating physical models to forecast performance.

3

SEMICONDUCTOR PHYSICS

Semiconductors such as gallium nitride (GaN), aluminum nitride (AlN), and indium nitride (InN) are classified as polar materials due to their inherent ionic sublattice displacements, which generate net macroscopic polarization. In their unstrained zinc-blende crystal configurations, these materials lack a net polarization because the symmetrical arrangement of cation and anion sublattices cancels out dipole moments. However, in wurtzite-structured crystals common in III-nitride semiconductors deviations from ideal atomic positions create spontaneous polarization.

Strain-induced piezoelectric polarization further contributes to net polarization in heterostructures through relative displacements between ion sublattices. In GaN-based quantum well systems, the combined effects of these polarization mechanisms produce strong internal electric fields. These fields lead to two critical phenomena:

1. **Interface charge accumulation** at III-nitride heterojunctions
2. **Reduced wavefunction overlap** between electrons and holes due to spatial segregation.

This fundamental behavior significantly impacts the performance and design of nitride-based optoelectronic devices.

3.1 Spontaneous and Piezoelectric Polarization

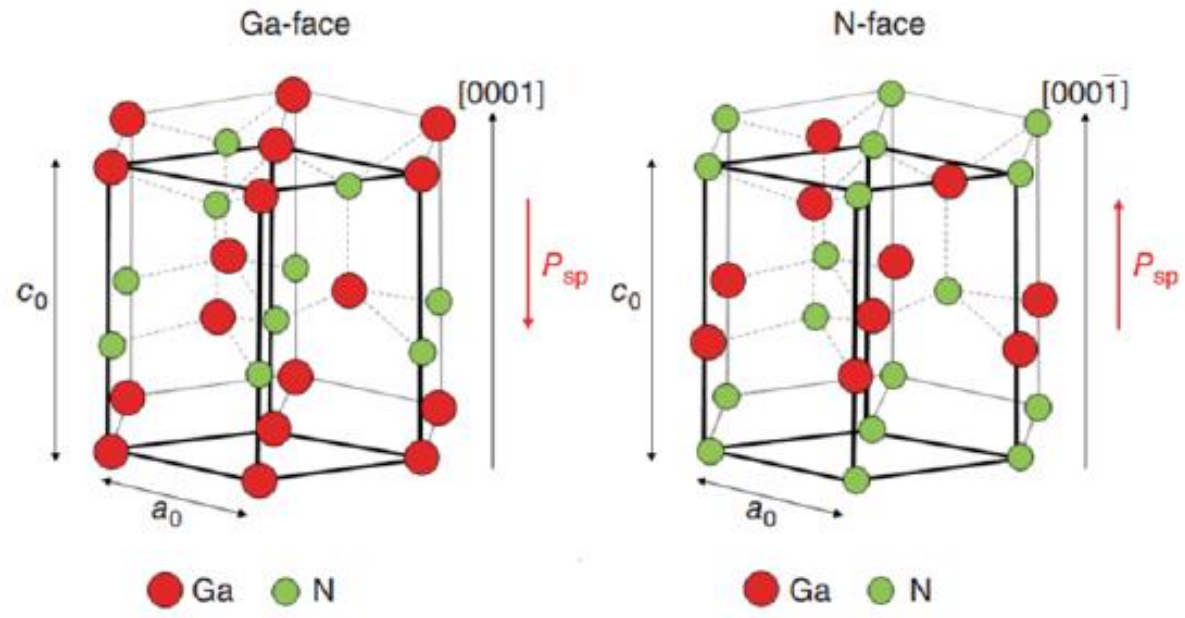


Figure 3.1: Crystal structure unit cell of GaN material for Ga-face and N-face

In compounds like GaN, atoms are arranged in a tetrahedral configuration, where each atom is bonded to four neighboring atoms. These bonds are predominantly covalent but have a significant ionic character due to the substantial difference in electronegativity between the metal (e.g., Ga) and nitrogen atoms. The higher electronegativity of nitrogen attracts electrons more strongly, increasing the ionic nature of the Ga-N bond compared to other III-V semiconductors.

This ionic character leads to a net polarization within the crystal, particularly in structures lacking inversion symmetry. In the case of wurtzite III-nitrides, this results in a spontaneous polarization along the c-axis, even in the absence of external strain. Although similar effects can occur in the direction of zinc-blende crystals like GaAs or InP, the lower ionicity in those materials makes the polarization much weaker.

Wurtzite GaN crystals exhibit two distinct polar surfaces: the Ga-face ([0001] direction) and the N-face ([0001] direction). The Ga-face can be visualized as having a gallium atom directly above a nitrogen atom, while the N-face is the reverse. When growing thin films heteroepitaxially, the polarity of the resulting material cannot be easily predicted and must be determined experimentally.

The wurtzite lattice is characterized by three key parameters: the bond length ratio (u_0) between cations and anions, the lattice height (c_0), and the edge length of the basal hexagon (a_0). These parameters refer to the equilibrium state of the lattice, as indicated by the subscript “0”.

The degree of spontaneous polarization is influenced not only by the ionic charge of the covalent bond but also because of the non-ideality of the crystal lattice. The spontaneous polarization of III-nitrides is mainly caused by the extremely ionic covalent bond parallel to the c-axis however, the tetrahedral structure's other three covalent bonds are similarly ionic.

Parameter	AlN	GaN	LnN
a0	3.112	3.189	3.54
c0	4.982	5.185	5.705
u0	0.380	0.376	0.377
c0/a0	1.6010	1.6259	1.6116
PSP [C/m2]	-0.081	-0.029	-0.032
C13[GPa]	108	103	121
C33[GPa]	373	405	182
e33[C/m2]	1.46	0.73	0.97
e31[C/m2]	-0.60	-0.49	-0.57

Table3.1: Lattice parameters III-nitrides at 300 K

Because of the high ionicity of the metal-nitrogen covalent connection, the polarization of the crystal will change significantly if the ideality of the III-nitride lattices is altered externally. Strain is one method of altering the crystal lattice's ideality. The ideal lattice parameters c0 and a0 of the crystal structure will alter to accommodate stress if it is applied to the III-nitride lattice. As a result, the degree of polarization will vary. Piezoelectric polarization is the term for this extra polarization in strained III-nitride crystals.

[8] PSP = PSPz is the spontaneous polarization along the wurtzite crystal's c-axis. Using the piezoelectric coefficients e_{33} and e_{13} (found in table 3.1), the piezoelectric polarization can be computed as follows:

$$P_{PE} = e_{33}\epsilon_z + e_{31}(\epsilon_x + \epsilon_y) \tag{3.1}$$

If ϵx and ϵy represent the in-plane strain and ϵz represents the strain along the c-axis:

$$\epsilon_z = \frac{c-c0}{c0} \tag{3.2}$$

$$\epsilon_x = \epsilon_y = \frac{a-a0}{a0} \tag{3.3}$$

The relation between the a0 and c0 of the hexagonal *GaN* is given to :

$$\frac{c-c0}{c0} = -2\frac{C13\ .\ a-a0}{C33\ .\ a0} \tag{3.4}$$

where the elastic constants C_{13} and C_{33} are found in table 3.1. The quantity of piezoelectric polarization in the c-axis direction can be calculated using equations 3.2 and 3.4.

$$P_{PE} = 2\frac{a-a0}{a0}\left(e31 - e33\ \ \frac{C13}{C33}\right) \tag{3.5}$$

Due to the fact that [e31 − e33(C13/C33)] < 0, the piezoelectric polarization is negative for tensile strained barriers and positive for compressive strained barriers for all AlGaN compositions. Since the spontaneous polarization for GaN and AlN was discovered to be negative, the spontaneous polarization for Ga(Al)-face heterostructures is oriented towards the substrate, as illustrated in figure 3.3

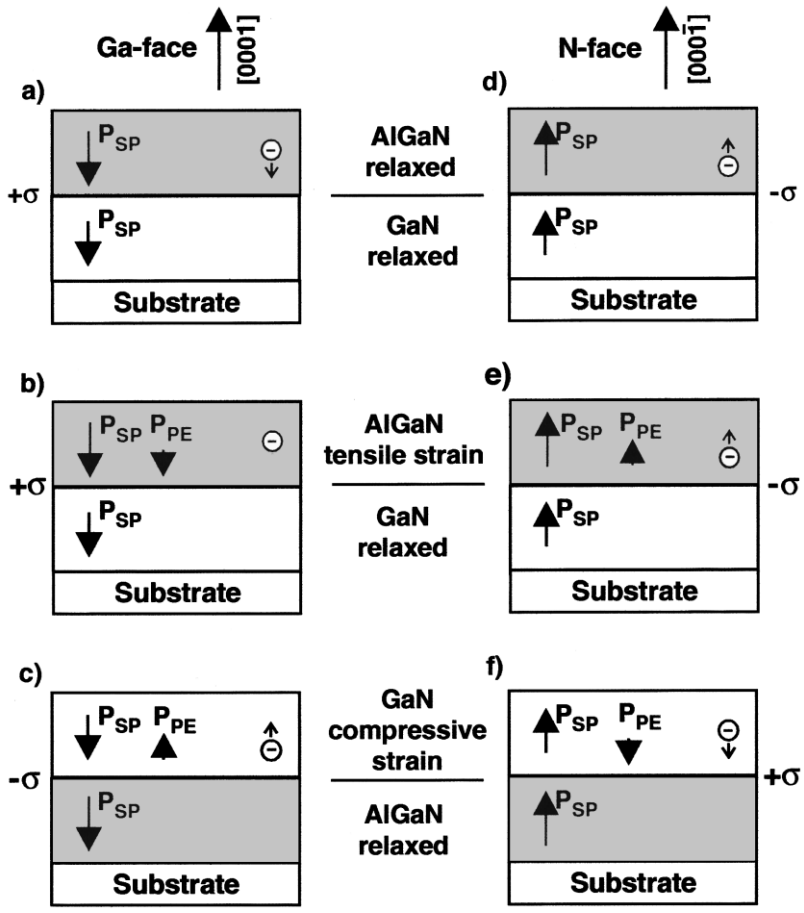


Figure3.2: Directions of polarization and polarization-induced sheet charge density

Hence, in the case of compressively stressed top layers, the alignment of the piezoelectric and spontaneous polarization is anti-parallel, whereas in the case of tensile strain, it is parallel. Both the spontaneous polarization and the piezoelectric material alter their sign if the polarity shifts from Ga-face to N-face.

3.2 Charge density

In figure. 3.3 as an example to calculate the charge density. $\rho P = \nabla P$ is the polarization induced charge density associated with a gradient of polarization in space. Similarly, the polarization of a bilayer can either rise or decrease at an abrupt interface of a top/bottom layer (AlGaN/GaN or GaN/AlGaN) heterostructure, resulting in a polarization sheet charge density specified by

$$\sigma = P(t) - P(b) = P_{SP}(t) + P_{PE}(t) - P_{SP}(b) - P_{PE}(b) \tag{3.6}$$

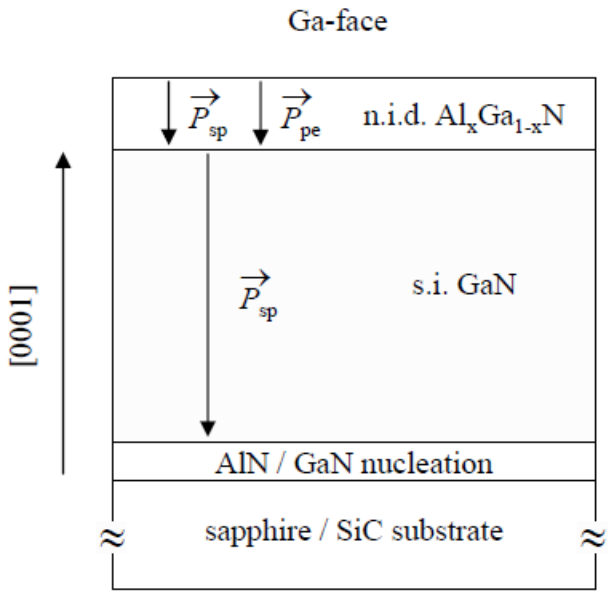


Figure 3.3: Polarization vector directions for an AlGaN/GaN

Variations in material composition, surface irregularities, or strain distribution can influence the local profile of the polarization-induced sheet charge density. However, the total charge associated with polarization across the interface typically remains comparable to that at an ideal, abrupt junction. When the polarization-induced sheet charge is positive (+σ), it tends to attract free electrons, which compensate for the charge imbalance.

Provided the interface is relatively smooth and the band offset between AlGaN and GaN is sufficiently large, these electrons accumulate to form a two-dimensional electron gas (2DEG) with a defined sheet carrier concentration (ns). Conversely, a negative sheet charge density (−σ) would lead to the accumulation of holes at the interface.

The polarization-induced sheet charge for an AlGaN with a Ga(Al)-face on top of a GaN heterostructure is positive (Figure. 3.2a). Because GaN and AlGaN spontaneous polarization differ, electrons will be trapped at the interface even if the heterostructure is relaxed (AlGaN thickness > 65 nm). The difference between PSP (AlGaN) and PSP (GaN), as well as the sheet charge and sheet carrier concentration, will rise if this heterostructure grows pseudomorphically (Fig.3.2b) due to the piezoelectric polarization of the tensile strained AlGaN barrier. In contrast to the Ga-face structure, the spontaneous and piezoelectric polarizations in N-face AlGaN/GaN heterostructures point in opposite directions. At this interface, holes may accumulate due to the negative polarization-induced sheet charge (Figures. 3.2d and 3.2e).

Physical properties of GaN and AlN:

Lattice constant:

$$a(x) = (-0.77x + 3.189) \cdot 10^{-10}\,[m] \tag{3.7}$$

Elastic constants:

$$C13(x) = (5x + 103)[GPa] \tag{3.8}$$

$$C33(x) = (-32x + 405)[GPa] \tag{3.9}$$

Piezoelectric constants

$$e31(x) = (-0.11x - 0.49)[C/m^2] \tag{3.10}$$

$$e33(x) = (-0.73x + 0.77)[C/m^2] \tag{3.11}$$

Spontaneous polarization

$$PSP\,(x) = (-0.052x - 0.029)[C/m^2] \tag{3.12}$$

Equations (2.6), (2.7), and (2.13) are used to determine the quantity of the polarization-induced sheet charge density

$$|\sigma| = |PPE(Al_xGa_{1-x}N) + PSP\ (Al_xGa_{1-x}N)\ - PSP\ (GaN)| \tag{3.13}$$

$$|\sigma| = 2\frac{a(0)-a(x)}{a(x)}\left\{ e31(x) - e33(x)\frac{C13(x)}{C33(x)}\right\} + PSP(x) - PSP(0) \tag{3.14}$$

Sheet charge density (ns):

$$ns(x) = \frac{+\sigma\ (x)}{e} - \left(\frac{\epsilon 0\epsilon(x)}{de^2}\right)(e\Phi b(x) + EF\ (x) - \Delta EC(x)) \tag{3.15}$$

where EF is the Fermi level in relation to the GaN conduction-band-edge energy, d is the AlGaN barrier width, eΦb(x) is the Schottky Barrier of the gate contact, and ΔEC(x) is the conduction band offset at the AlGaN/GaN interface. Using the polarization induced sheet charge density from eq. 3.15, we calculate the sheet carrier concentration using the following approximations:

Dielectric constant:

$$\epsilon(x) = -0.5x + 9.5 \tag{3.16}$$

Shottky barrier:

$$e\Phi b(x) = 1.3x + 0.84[eV] \tag{3.17}$$

Fermi energy:

$$E_F\ (x) = E0(x) + \frac{\pi h^2}{2\ \pi\ m^*(x)}\ ns(x) \tag{3.18}$$

$E0$ is given by

$$E_0(x) = \left\{ \frac{9he^2}{8\pi\epsilon 0\sqrt{8m^*(x)}} \quad \frac{ns(x)}{\epsilon(x)}\right\}.1^{\frac{2}{3}} \tag{3.19}$$

Assuming a constant surface barrier, the 2DEG sheet charge density can be computed as a function of either the barrier layer thickness or the composition of the Al alloy.

The computed 2DEG density as a function of the Al alloy composition, with the AlGaN barrier thickness as a parameter, is displayed in Figure 3.4. Furthermore, as a reference, the bound polarization induced sheet charge (σ = σ2DEG) is displayed.

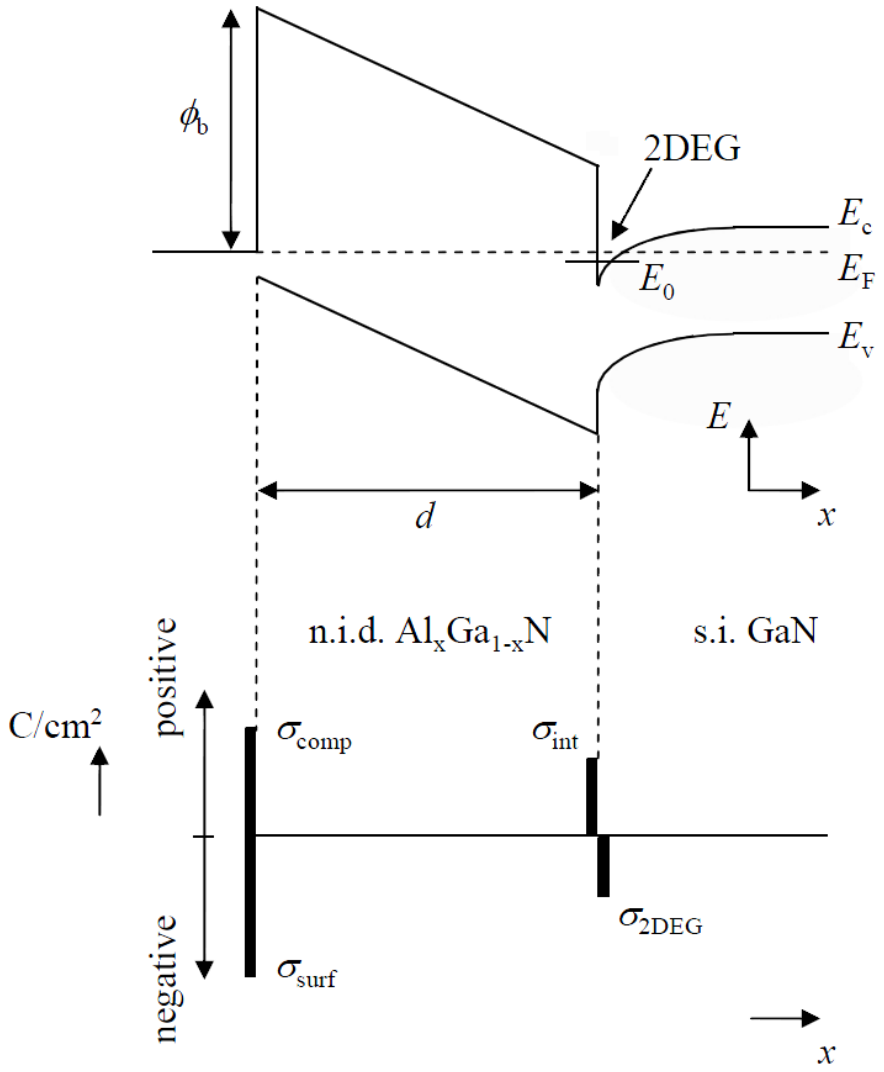


Figure 3.5 An energy band diagram showing the bound and compensatory mobile sheet charge densities caused by polarization in a undoped AlGaN/GaN heterostructure

Figure illustrates a typical AlGaN/GaN heterostructure's band diagram and relative charge placement. The region surrounding the contact displays a negative charge (σsurf),

while the GaN buffer layer displays a second negative charge (σ2DEG), which is the source of the 2DEG. Due to the carrier's spatial separation from dopants in the barrier layer, these electrons are more mobile than electrons in the active layer's bulk. From the perspective of a bands diagram, the presence of 2DEG is evident since the conduction band of GaN near the AlGaN layer crosses the Fermi level, indicating that a significant number of electrons are stored there. To optimize the performance of AlGaN/GaN HFETs, the electron source must be understood and controlled. However, nothing is now understood about the issue.The presence of surface donor-like states in the AlGaN layer is one potential outcome. It should be mentioned that these two layers are required to supply the electrons that comprise the compensating mobile sheet charge density (σ2DEG) when the investigated AlGaN/GaN structures are undoped. Interactions with the environment or dangling bonds may have contributed to this surface positive charge.

[9] Thermally produced electrons in the buffer cannot be the cause of the 2DEG because they must leave a +ve space charge behind. As the charge should have the smallest magnitude possible in a well-designed FET, it is acceptable to entirely disregard it for the sake of clarity and the Fermi level is located at the GaN conduction band lower edge. Similar to how donors in the AlGaN barrier can produce the 2DEG, A positive surface charge must be generated in the GaN by electron transfer from donor-like surface states into lower energy empty states.

Nevertheless, electrons must shift into acceptor-like surface states at the expense of the 2DEG in order for there to be any negative surface charge. In other words, the total number of electrons in the 2DEG plus the number of ionized donor-like states on the surface equals the number of ionized donors in the AlGaN layer.

The 2DEG population does not grow proportionately at the barrier thickness, however, as no 2DEG population growth has been seen and strain relaxation begins at a certain value.

At low AlGaN thickness levels, they anticipate that all of the donor-like surface states will be occupied, and that they are situated very deep in the AlGaN band gap. There won't be any 2DEG since the polarization-induced charges will control the field in the top layer. As the AlGaN layer's width expands, the surface Fermi level moves in the direction of the deep donor level. They begin to empty as soon as the Fermi level reaches the surface states.

A 2DEG may then arise at the AlGaN/GaN contact as a result of the field in the AlGaN barrier being reduced.

3.3 Normally Off transistor

Enhancement-mode GaN high-electron-mobility transistors (HEMTs) are critical for power switching applications due to their fail-safe operation and simplified gate drive requirements, while depletion-mode AlGaN/GaN HEMTs remain prevalent in high-frequency systems89. Achieving normally-off operation involves multiple engineering approaches:

Key Methods for Normally-Off Operation

1. **AlGaN Barrier Recessing**

Localized plasma etching of the AlGaN layer beneath the gate reduces 2DEG density, requiring precise etch depth control 35. Challenges include gate leakage currents and threshold voltage (Vth) variability due to surface damage. Advanced techniques like multi-layer AlGaN heterostructures improve Vth uniformity while maintaining low on-resistance (Ron).

2. **Fluorine Plasma Treatment**

Implanted F- ions under the gate deplete the 2DEG through negative charge injection, enabling positive Vth shifts[5]. However, thermal instability during high-temperature processing limits reliability.

3. **Hybrid MISHEMT Configuration**

Complete removal of the AlGaN barrier under the gate and replacement with a dielectric layer (e.g., Al2O3) combines MIS gate control with 2DEG conduction 34. Dielectric choice critically impacts channel mobility and Vth hysteresis.

4. **p-GaN Gate Technology**

Industry-adopted approach where Mg-doped p-GaN layers elevate the conduction band at the AlGaN/GaN interface, depleting 2DEG at zero bias (Figure 3.6)14. Key considerations include:

- Selective etching of p-GaN to define gate regions

- Mg dopant diffusion into AlGaN during processing
- Charge compensation at the p-GaN/AlGaN interface

Device Physics and Challenges

The energy band structure shows Schottky contact-induced depletion at the metal/p-GaN interface, with partial neutral regions in sufficiently thick p-GaN layers. Polarization-induced electric fields govern 2DEG formation, which remains suppressed under zero gate bias due to Fermi level positioning below the conduction band45. Positive gate bias realigns energy bands, restoring 2DEG conductivity when Vg exceeds Vth.

Critical reliability concerns include:

- Vth drift under high-temperature/stress conditions
- Dynamic Ron degradation from charge trapping
- Breakdown mechanisms at high drain/gate biases

This analysis highlights the intricate trade-offs between processing complexity, performance metrics, and reliability in developing commercially viable normally-off GaN HEMTs.

3.4 Traps in *GaN* and *AlGaN*

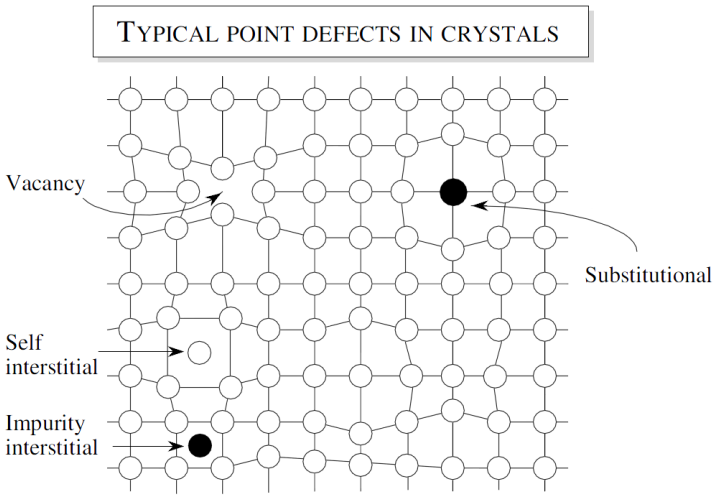


Figure 3.6 Point defect in crystal

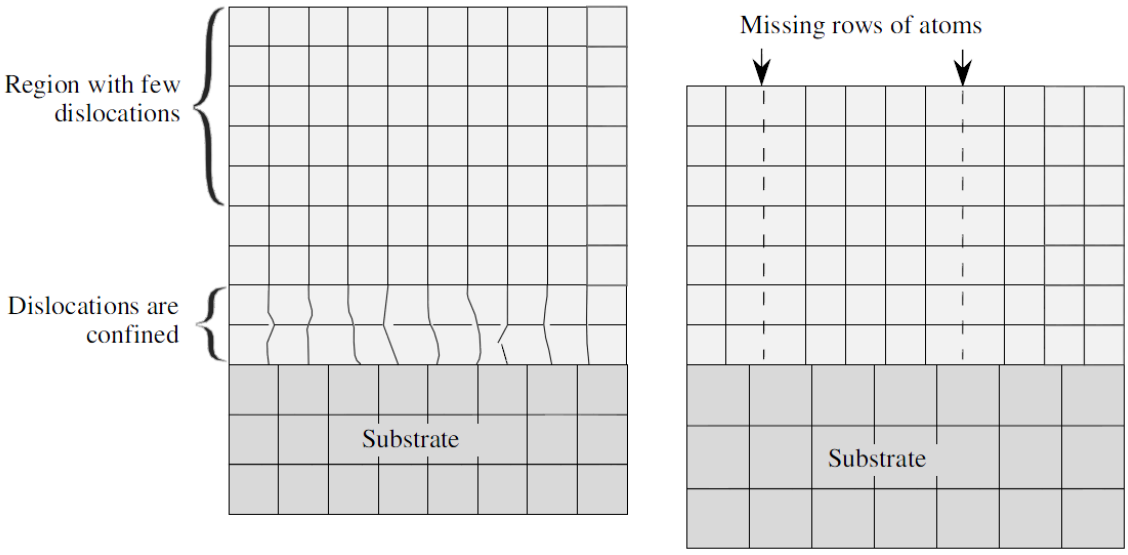


Figure 3.7 These figures illustrate the dislocations due to the overlayer substrate interface.

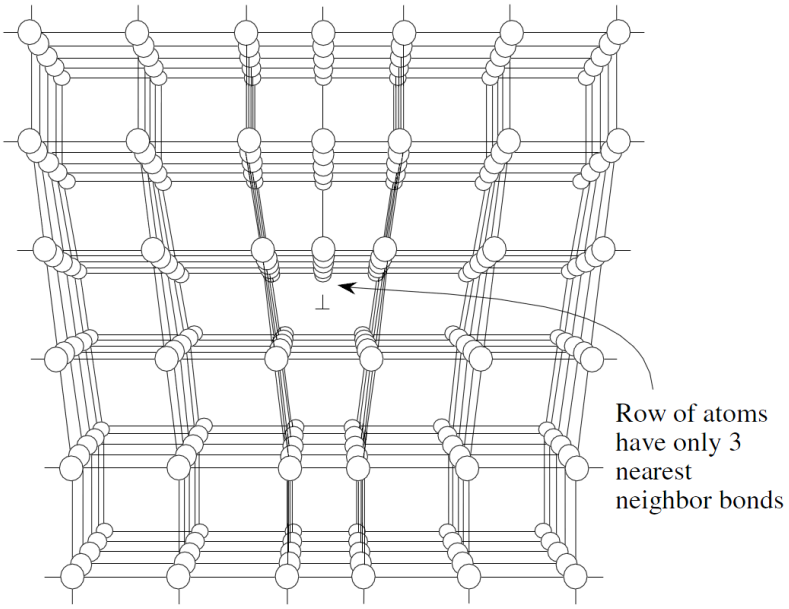


Figure 3.8 Volumetric dislocations

[2] In devices made using Wide band semiconductors, 2DEG electrons are trapped and detrapped both inside the layer structure and at the semiconductor surface. Current characteristics at RF frequencies are substantially less than those under DC conditions due

to the development of quasi-static charge distributions as a result of these trapping phenomena. Because of the DC output characteristics and the selected operation class, the device's microwave output power capability is thereafter much lower than anticipated. Understanding the energy and spatial locations of the traps is crucial, even though their existence significantly affects the device's performance.

Traps can form both inside the layer and in the heterointerface because the heteroepitaxy growth approach makes traps more likely to occur. The former type is the result of the material quality being faulty during the process. Instead, the latter type is brought on by the two semiconductors' different lattice constants, which means that the material grown on top must change its lattice parameter at one of the bottom materials, which leads to the development of defects (figure 2.10). Both varieties result in flaws like those seen in figure 2.11.

Furthermore, superficial donor traps that work similarly to positive superficial charges can be produced via dangling bonds. All of these traps affect device performance since the drain current drops, which is how the 2DEG is consumed. Later in this section, we will discuss this method. Since deep level traps can come from a range of sources, such as impurities, point defects, extended defects, and growth conditions, it must be admitted that the energy locations of the traps in GaN material are not well described in the literature, and even the reasons for their existence are not entirely clear. There aren't any detailed descriptions of the traps for this yet.

[4] Traps are frequently observed at interfaces in heterostructures due to abrupt changes in the lattice constant. Moreover, the GaN material that constitutes the top layer of the AlGaN exhibits a notable strain. The optical emission from this strain is intense at energies below 1.6 eV. In addition to the interfaces, traps are also there beneath the gate. [23], [24] High voltages result in the creation of considerable stresses inside GaN and AlGaN layers because of their strong piezoelectric nature. HEMT running at high voltage develops a strong electric field across the barrier beneath the gate. A very small portion of the AlGaN barrier may experience extremely high mechanical stress as a result. Moreover, AlGaN on GaN usually undergoes considerable tensile strain because to their lattice mismatch, which causes a significant amount of elastic energy to be stored at rest.

3.5 Electrothermal Stress

Trap states are created and activated in different layers of AlGaN/GaN High Electron Mobility Transistors (HEMTs) as a result of electrothermal stress. By resulting in phenomena including current collapse, threshold voltage shifts, and higher on-resistance, these traps can impair performance. A thorough layer-by-layer examination of trap formation brought on by electrothermal stress is provided below:

Passivation Layer

Charge injection into surface states or defects at the semiconductor/passivation interface can be brought on by high electric fields and high temperatures. Additional trap sites may be introduced by surface pollution or oxidation that is made worse by heat stress. Current collapse and an increase in on-resistance can result from trapped charges modulating the electric field distribution.

AlGaN Barrier Layer

Defects and dislocations produced during epitaxial growth may serve as trap centers. These flaws may become active in response to electrothermal stress, creating trap states inside the barrier layer. Carrier density and mobility can be decreased by trapping carriers from the 2DEG in the barrier layer.

AlGaN/GaN Interface

Defects and rough surfaces can create trap states. Electrothermal stress can make these problems worse by encouraging defect migration or interdiffusion. Electrons from the 2DEG may be trapped at the interface, resulting in threshold voltage instability and current collapse.

GaN Channel Layer

Impurity complexes or point defects like nitrogen vacancies can function as deep-level traps. These traps can be activated or new traps can be created by electrothermal stress. Current deterioration and decreased carrier mobility can result from channel trapping.

For modelling of electrothermal effect I have introduced deep level traps in barrier layer, interface of AlGaN/GaN and GaN channel.

To replicate the behavior of electron traps frequently seen in experimental investigations, acceptor-type traps were created with energy levels determined in relation to the conduction band. In the vicinity of the AlGaN/GaN interface, where defect activity is enhanced by electric field crowding and thermally induced processes, the traps were thought to have a Gaussian spatial distribution. To represent common deep-level trap interactions, capture cross-sections for both electrons and holes.

A non-local tunneling model was used to accurately replicate TAT, allowing hole injection from the p-GaN gate into the trap states and electron tunneling from the channel. Multiphonon emission characteristics, such as a phonon energy of 91 meV and a Huang-Rhys factor of 20, which are indicative of GaN optical phonons, were used to further improve the trap-assisted recombination dynamics. Together, these parameters allow the simulation to reproduce current collapse and leakage currents that have been observed experimentally. These phenomena are known to result from trap activation under conditions of coupled high electric field and self-heating stress.

4

HEMT STRUCTURE

4.1 Structural details

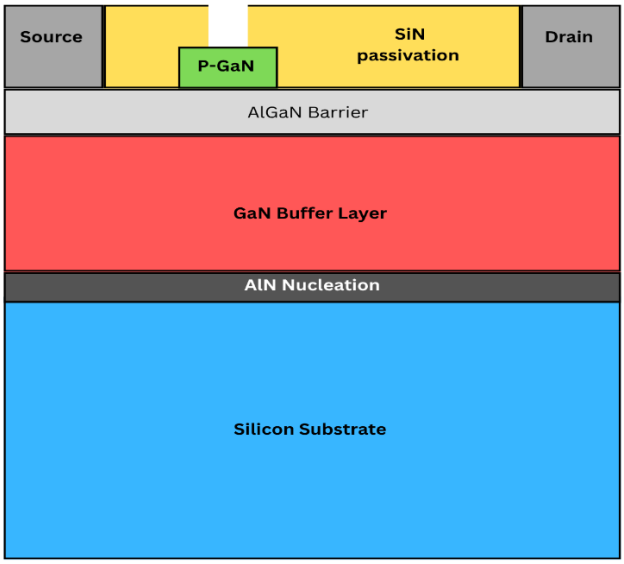


Figure 3.1 P-GaN HEMT Structure

The work of I. Hwang et al. [26], which showed a high-performance GaN-based HEMT with tungsten gate metal, served as the primary source of the structural and dimensional specifications for the suggested p-GaN gate HEMT device. Because of its applicability and shown efficacy in attaining high threshold voltage(Vth) and low gate leakage current two crucial performance criteria for enhancement-mode GaN transistors this study was chosen as a reference. A realistic and experimentally verified baseline for device behavior is guaranteed by matching the critical layer dimensions such as the gate length, p-GaN thickness, AlGaN barrier thickness, and overall device geometry with those reported by Hwang et al.

The key geometry parameters in the lateral direction of the device are:

- 4 μm p-GaN region width
- 2 μm gate contact width on p-GaN region
- 2 μm gate to source space
- 12 μm gate to drain space

4.2 Substrate (5 μm silicon substrate layer)

Unwanted The heteroepitaxial technique is used to grow the majority of GaN HEMTs. GaN layers are produced for device applications via Hydride Vapor Phase

Epitaxy (HVPE), MOCVD, and MBE. A few disadvantages of each technique include differing levels of surface roughness and epilayer quality. One of the major challenge to GaN is the absence of a substrate material that is both thermally compatible and lattice-matched (chapter 2). In our experiment we are using silicon as a substrate to overcome the lattice mismatch problem we are using a Nucleation layer of AlN . 5 μm silicon substrate layer

4.3 Nucleation layer (0.15 μm AlN nucleation layer)

This layer has an impact on the caliber of later layers' growth. The nucleation layer establishes the polarity of the buffer layer that follows [1]. AlN or GaN are frequently used as the nucleation layer. It lessens strain-induced flaws between substrates and succeeding layers and accounts for lattice mismatch. It serves as the buffer layer's seed layer.

4.4 Buffer layer (3 μm GaN buffer layer)

Together with the nucleation layer, this layer divides the active layer from the substrate. Because it is composed of a thick layer of GaN, it improves the quality of the material and plays a key role in electron transport. The 2DEG serves as a conduit for current flow and is situated along the border in the upper portion of this layer (shown in figure 3.1.1). There is a significant risk of creating flaws and traps when growing this epitaxial layer with MOCVD, which may be the main cause of performance deterioration.

As previously stated, three distinct substrates are used to build the HEMT devices specifically: SiC, Si, and Sapphire. Each of the three substrates in this study has a different buffer layer. The smallest lattice constant mismatch, at 4%, and thermal expansion coefficient mismatch, at 3.2%, are found between the SiC substrate and GaN. As a result, only a few nanometers of buffer layer thickness are needed for compensation. Nonetheless, there is a significant lattice mismatch between Si (17%) and Sapphire (16%) with GaN. A thicker buffer layer is necessary to prevent dislocation faults and compensate for strain. For Si and sapphire, the buffer's thickness is normally around 1 μm.

4.5 Barrier layer(15 nm AlGaN barrier layer)

An undoped AlGaN layer makes up this structure. The polarization effect causes this layer to supply electrons to the 2DEG. AlGaN with the right thickness can both encourage

2DEG confinement and stop electrons from leaking into the buffer layer. Consequently, the barrier layer increases the onto-off ratio and decreases leakage current (Ioff). Additionally, it enhances dynamic on-resistance and lessens the trapping effect. However, by increasing surface traps, excessively thick AlGaN can lower performance [21]. This layer is normally around 20 nm thick.

4.6 P-GaN layer (100 nm p-GaN layer for the gate region)

To achieve normally-off operation, which is essential for the dependability and safety of power electronic systems, a p-type gallium nitride (p-GaN or PGaN) layer has been integrated into high electron mobility transistors (HEMTs) in recent years. In order to introduce holes as the majority carriers, the PGaN layer is usually formed on top of the AlGaN barrier and doped with acceptor impurities, most frequently magnesium (Mg). The high activation energy of Mg in GaN (~150–200 meV), which implies that only a small fraction of the dopant atoms become ionized at ambient temperature, makes it difficult to achieve efficient p-type doping in GaN.

Nevertheless, a depletion area that inhibits the production of the two-dimensional electron gas (under the gate at zero gate bias can still be produced by incorporating a thick enough and suitably doped p-GaN layer. Because of this structure, the device will always be off by default and will only switch on when a positive gate voltage is supplied. A major drawback of traditional depletion-mode GaN HEMTs, which are normally on and need extra circuitry to assure safe operation, is addressed by the inclusion of a PGaN gate. PGaN-gated HEMTs are ideal for high-performance power conversion and radio frequency applications because they combine the advantages of high breakdown voltage, quick switching speed, and enhanced thermal stability.

4.7 Gate contact

The two most often used gate stacks in GaN HEMTs are Schottky and MIS (Metal-Insulator-Semiconductor). MIS stacks have less leakage current than Schottky stacks because of the extra insulator layer, but they also have less transconductance, or the channel's gate control. Al2O3, SiNx, and SiO2 are the most often utilized insulators in MIS, and Ni/Au is a frequent gate stack for Schottky gates.

It can also be advantageous to have a cap layer (AlN or GaN) on AlGaN. Using an AlN cap layer can result in a significantly lower gate leakage current and a greater drain current. However, the off-state current is roughly the same when AlN material is used in place of a GaN-based cap layer.

4.8 Source and drain contact

Usually, they are ohmic contacts. A non-rectifying low resistance connection known as the ohmic contact permits current to go from a metal to a semiconductor and back again. Theoretically, the applied voltage should cause the current to increase or decrease linearly. Ohmic connections are formed when the metal's work function is greater than that of the p-type semiconductor. This guarantees the least amount of resistance while making touch with 2DEG. The source and drain contacts for HEMTs are of the same kind.

4.9 Passivation layer (200 nm SiN passivation layer)

A variety of deeper traps are the source of the so-called "current collapse." Degradation of drain current at increasing bias voltages is known as current collapse. The surface passivation layer can effectively minimize this. Dielectric films such as SiO2, Si_xN_{1-x}, AlN, Al2O3, etc. are used for surface passivation in semiconductor devices to achieve stability and dependability. It has been asserted that the relatively low state density at the SiN/III-N interface in GaN HEMTs makes the SiN-based passivation technique effective in reducing current collapse.

5

HEMTS SIMULATIONS

Simulation activities can be carried out using particular programs that attempt to replicate the actual behavior of a device. To simulate HEMT devices produced using GaN and AlGaN materials, I used Sentaurus, a TCAD simulator offered by Synopsys.

5.1 Device structure

For this study, the device structure and dimensions were adopted from a previously published GaN HEMT design, as referenced in [26]. Building on this established geometry, additional trap states were introduced into the simulation to analyze their impact on device performance. Specifically, interface traps were incorporated at the AlGaN/GaN heterojunction, and bulk traps were modeled within the GaN buffer layer. This approach enabled a detailed investigation of trap-related phenomena such as current collapse and threshold voltage shifts. The inclusion of these traps in the simulation framework provided insights into trap-assisted leakage mechanisms and their influence on ON-resistance degradation, closely reflecting behaviors observed in experimental measurements.

The device structure which is simulated is in fig 5.1

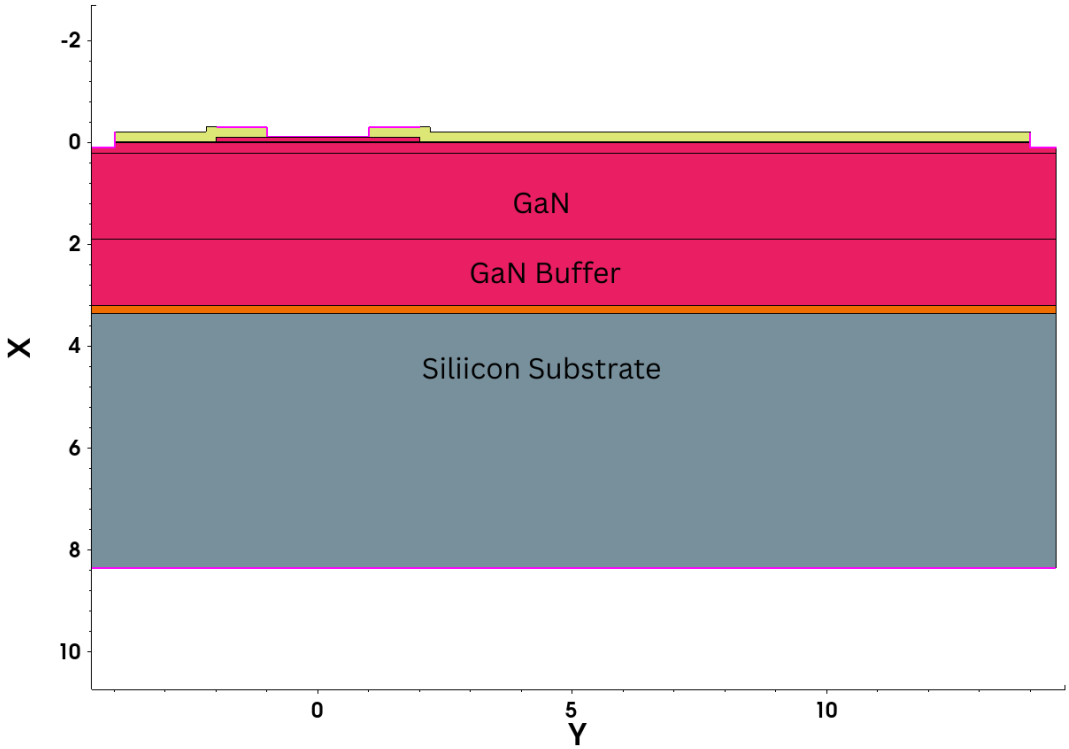


Figure : 5.1 Structure design in too

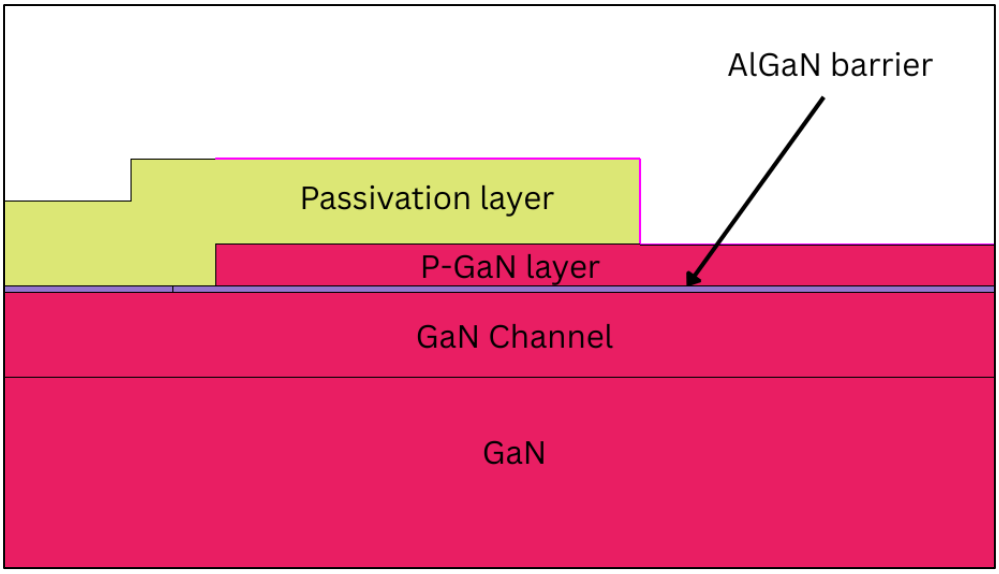


Figure 5.2 Showing the Barrier layer

The substrate is of Si, the nucleation layer in AlN, the buffer layer is GaN, the barrier layer is in AlGaN, the passivation layer on top of the device in Nitride, and the Drain and Source regions using the Synopsys Device Editor tool. Ultimately, I positioned the Gate, Drain, Source, and Substrate contacts, yielding the configuration depicted in Figure 5.3.

In order to assess the electrical behavior and the distribution of the physical parameters, such as the electric field, electron population, electrostatic potential, and so on, the next step was to construct a decent mesh. For this reason, it must be ensured that a tiny mesh covers any area exposed to high current, strong electric field, and sudden variations. Accordingly, a good mesh should be positioned in the 2DEG zone, which is the area of high current interest; in the areas with edges, which is the area of concentrated high electric field; and in the area where material changes occur.

Consequently, I acquired the mesh depicted in Figure 5.3 It is evident from the top perspective that the gadget has a thin mesh in the center and upper sections. The only reason for the center mesh is the modifications in the materials. A zoom of the gate region is shown in the bottom picture, where two distinct mesh types are present: one covering the gate edges and the thinner one for the 2DEG and material changes.

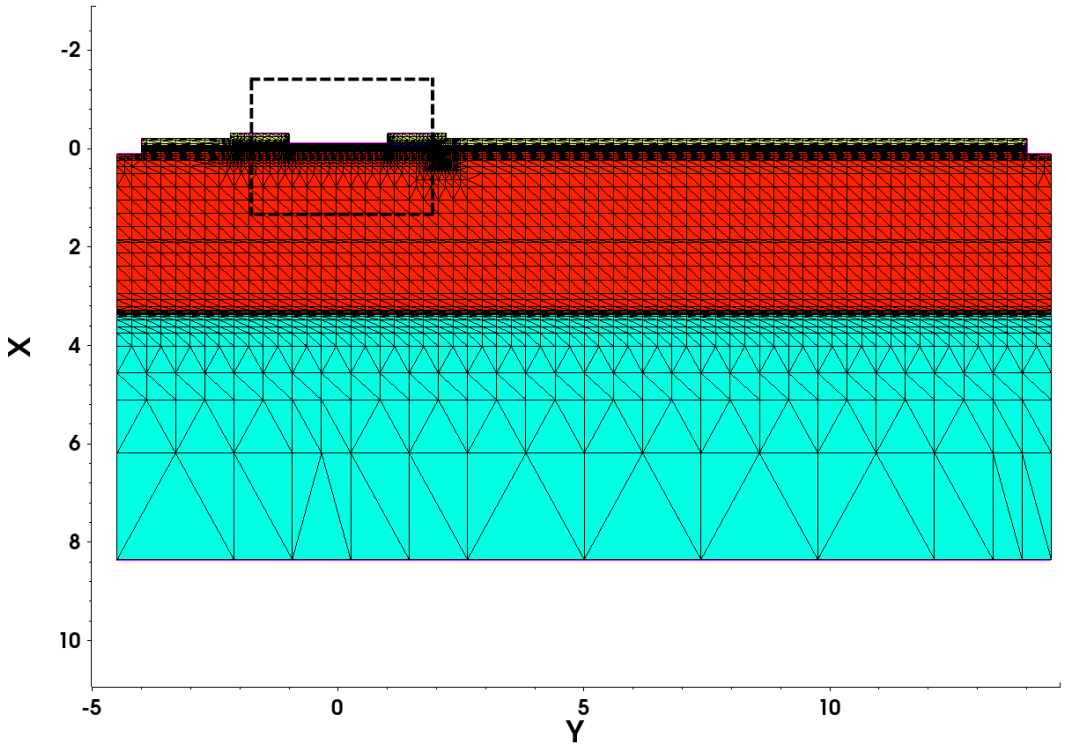


Figure 5.3 Changes in Meshing as per region and interfaces

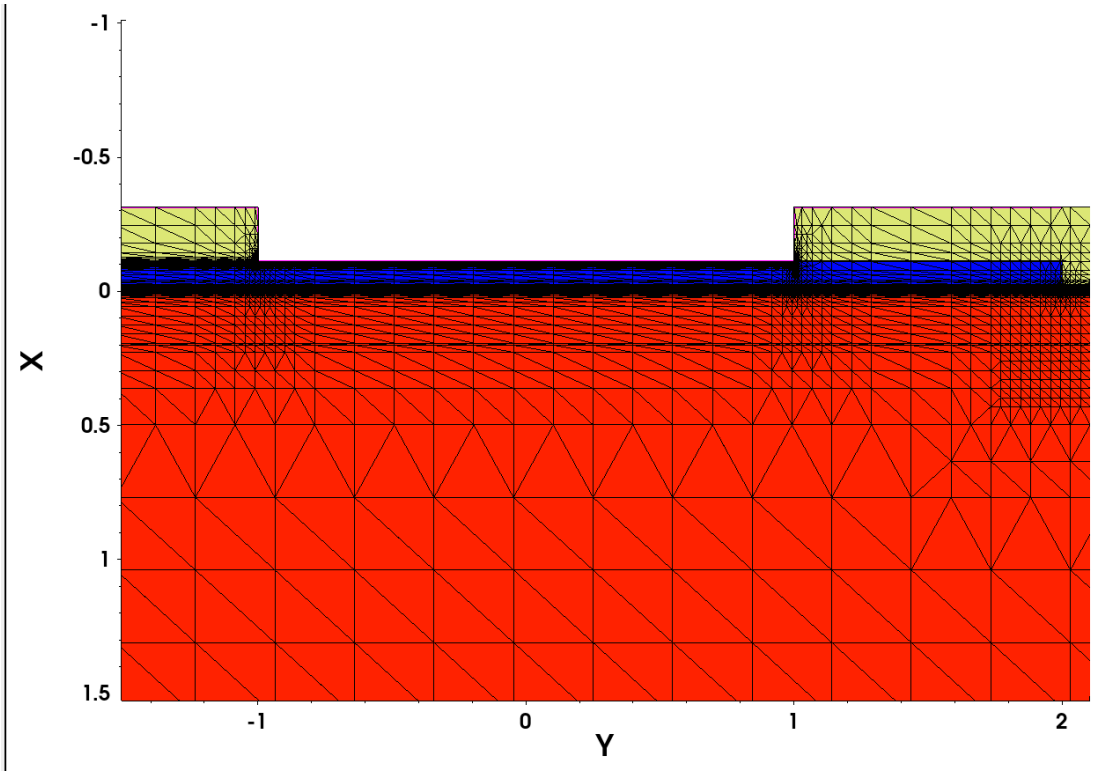


Figure 5.4 Denser meshing at channel layer and interfaces

5.2 Simulation setup

General Physics model used to simulate AlGaN / GaN hetrostructure a simplified strain-based piezoelectric polarization model.

- Generation and recombination: Shockley Read Hall (SRH), radiative, and Auger models. Avalanche models are used as required.
- Mobility: The Masetti mobility model accounts for doping-dependent mobility degradation. when the electric field in the device rises above Ecrit. To model the high-field saturation effects in GaN devices, the Caughey-Thomas formula is used.
- Fermi–Dirac statistics are used for the carrier concentration calculations. Thermionic boundary conditions are required at the heterointerfaces of the device.
- The incomplete ionization model accounts for the high ionization activation energy of magnesium in GaN.
- To model the TAT mechanism in the barrier layer, two nonlocal meshes are defined: one at the p-gate–barrier interface (NLM_Top) and one at the channel–barrier interface (NLM_Bot). The TAT current is primarily due to electrons tunneling from the channel region to the traps in the barrier, and holes tunneling from the p-gate valence band to the traps.

  Tunneling at the gate contact region is modeled by using eBarrierTunneling with the Band2Band option so as to capture electron tunneling between the GaN valence band and the metal conduction band In the Physics section, the models required to simulate the AlGaN and GaN heterostructure devices are defined. Due to the complexity of the device, considering several material interfaces and trap conditions across the device, polarization model activation and trap profiles are defined using region-wise, materialwise, and interface-wise Physics sections.
- For the GaN buffer, AlGaN buffer, and nucleation layers, a carbon doping of concentration 1×1019 cm–3 is defined as acceptor type with an energy level of –0.8 eV from the midbandgap.

Band diagram

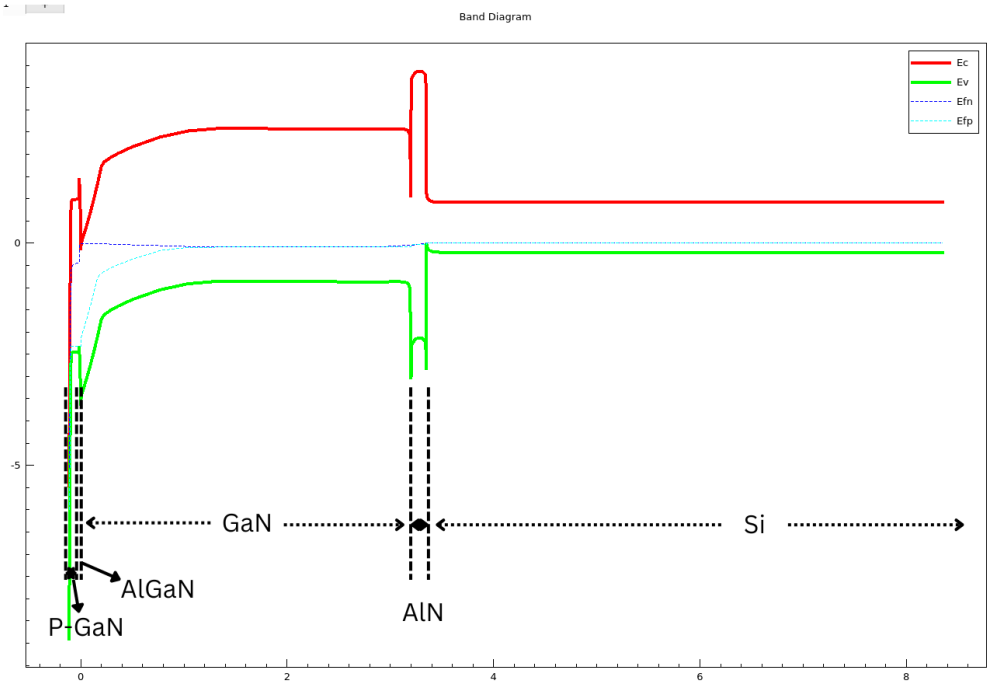


Figure 5.5 Energy Band Diagram schematics for zero bias

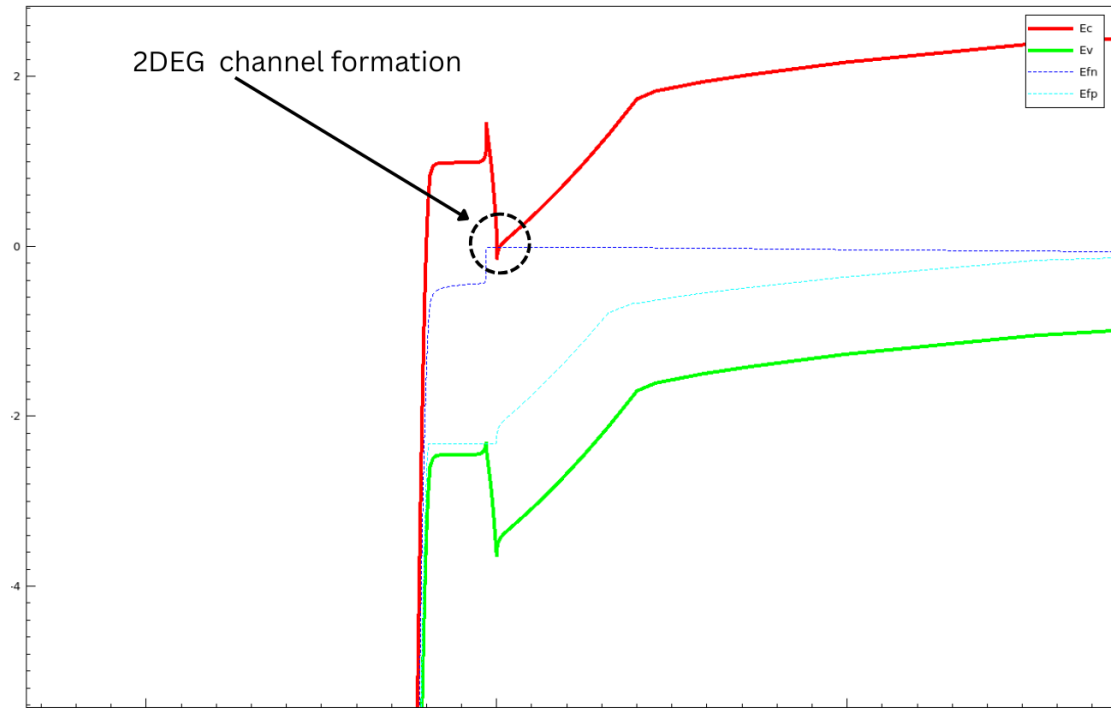


Figure 5.6 Energy Band Diagram showing 2DEG (Triangular Quantum well).

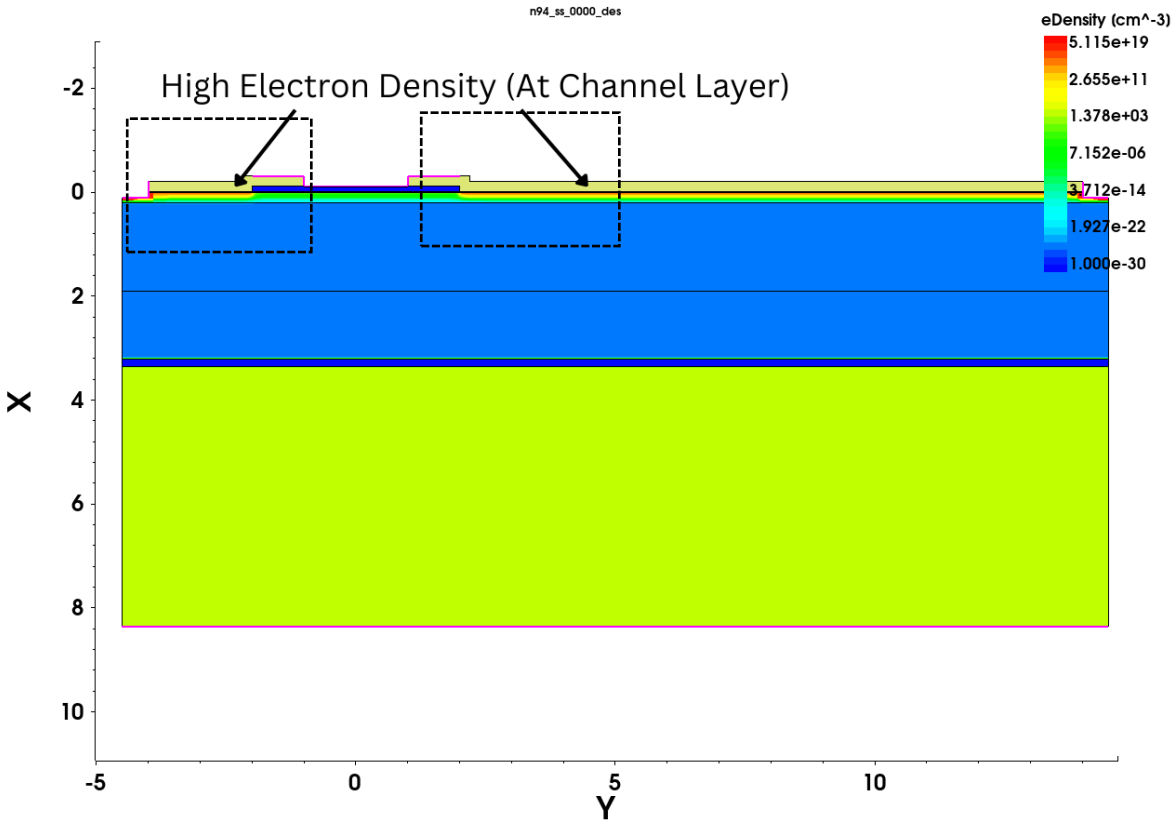


Figure 5.8 Show the Electron Density

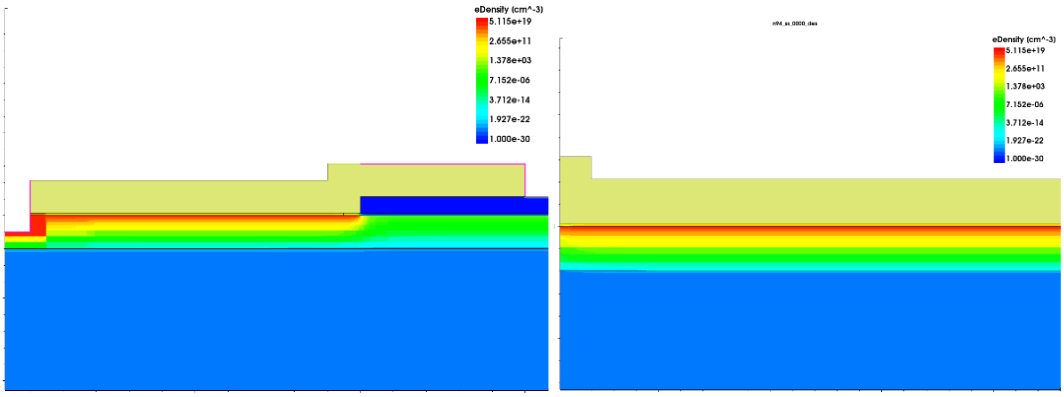


Figure 5.9: Showing the Density of Electrons at Channel region

Electron mobility at the channel layer

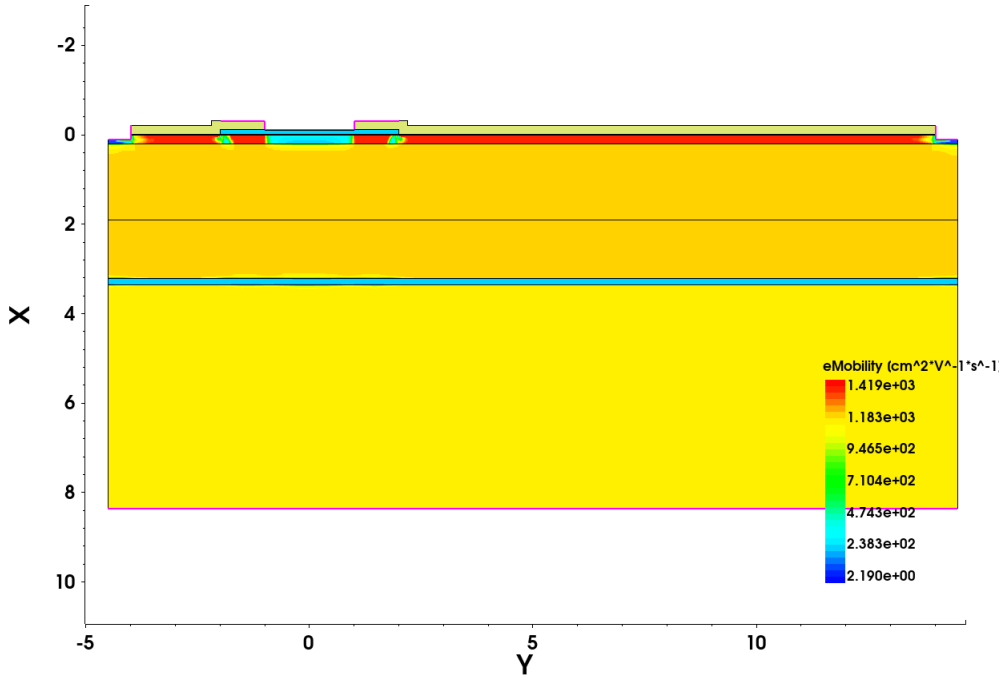


Figure 5.10 Shows the Electron Mobility

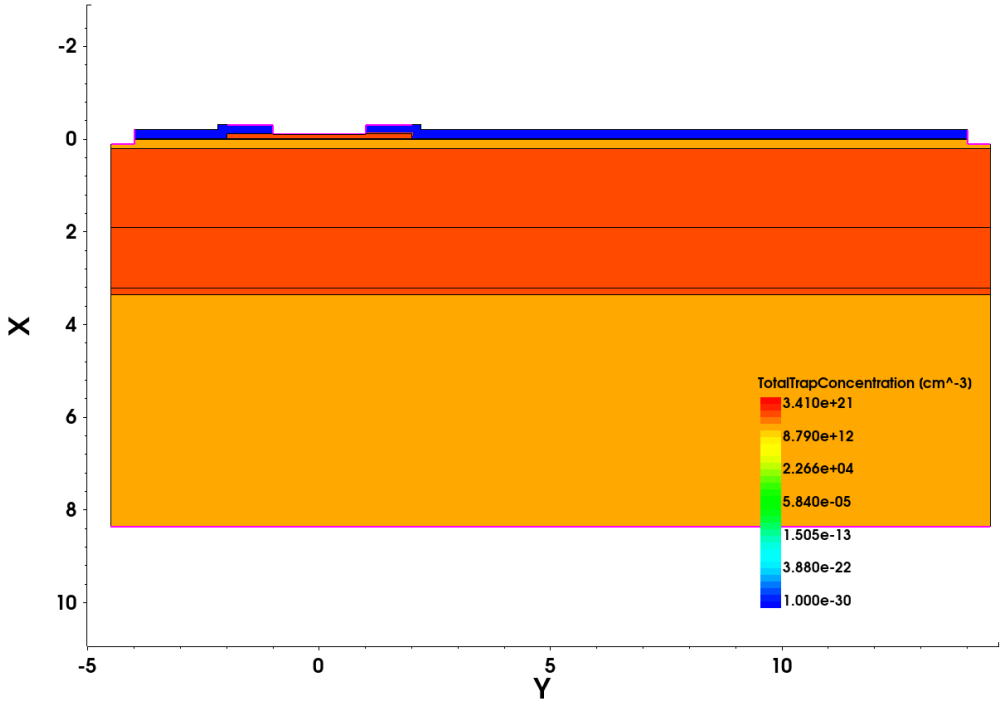


Figure 5.11 Shows the Total Trap Concentration

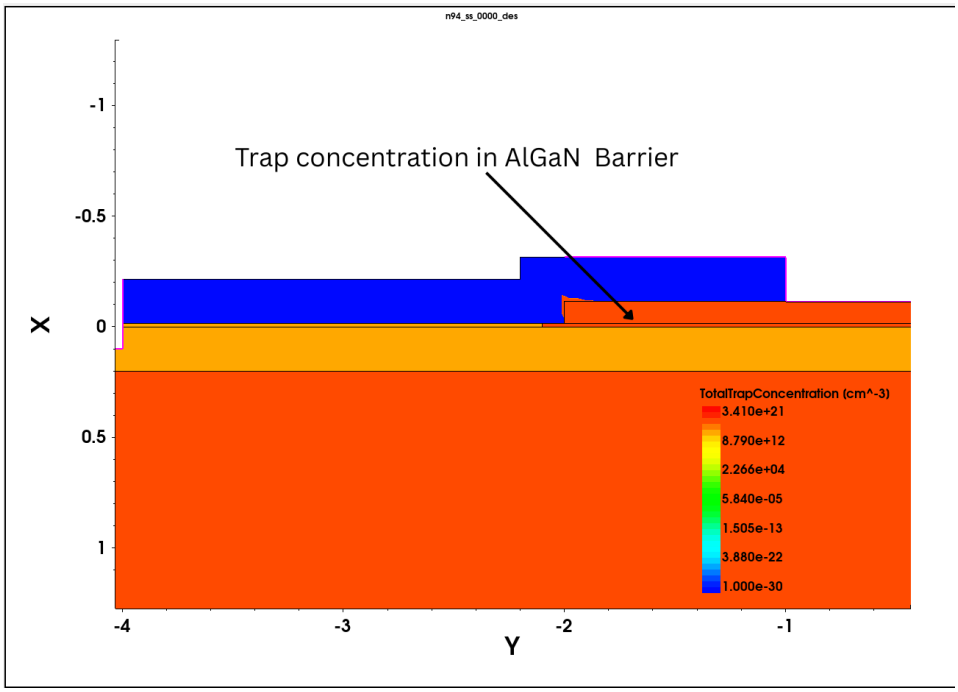


Figure 5.12 shows the Trap concentration in different layers.

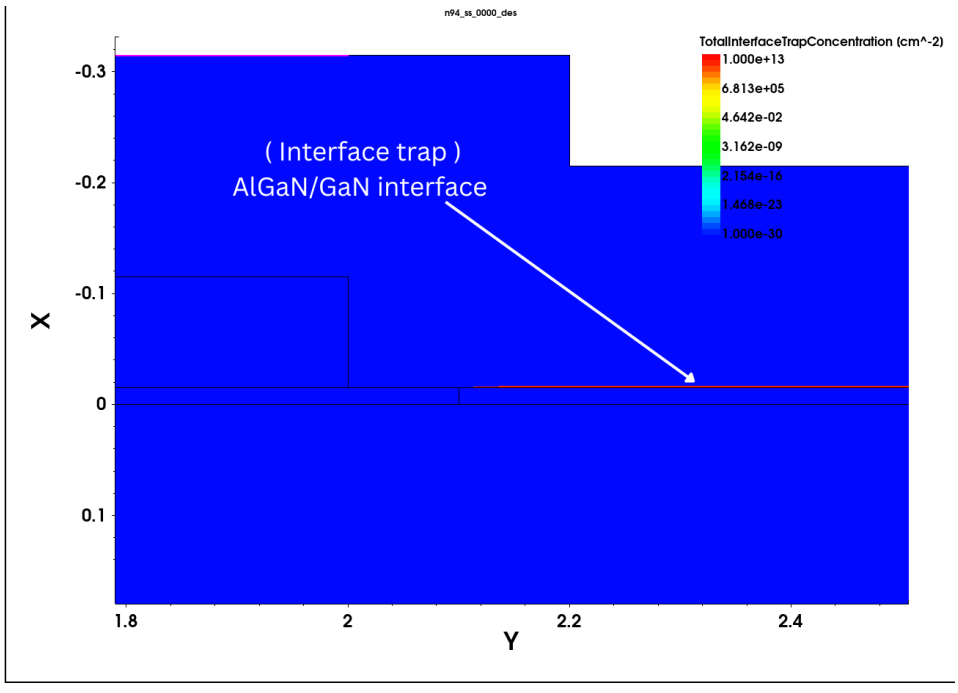


Figure 5.13 shows the Interface Trap concentration in Barrier layer.

5.3 DC simulations

A time-dependent transient analysis was used to model the AlGaN/GaN HEMT's electrical response under dynamic bias conditions. To create a physically consistent steady-state starting point, the simulation starts with a Poisson-only solution to stabilize the electrostatic potential profile. This is followed by a coupled Poisson–Electron–Hole solution.

To simulate actual device operation, a two-step transient bias ramping was then carried out. The 2DEG at the AlGaN/GaN interface was formed in the first stage by progressively increasing the gate volatge from 0 V to 6 V.

To guarantee convergence and numerical stability, the gate ramp was run using adaptive time-stepping across a simulated 1-second time interval. The channel construction and current conduction characteristics were recorded in the second stage by ramping the drain voltage from 0 V to 40 V throughout the course of the following second. Self-consistent solutions to Poisson and continuity equations controlled carrier movement during this stage. In order to evaluate carrier dynamics and possible trap-induced effects, the output drain current was displayed with a spatial resolution and recorded at regular intervals for post-processing.

In addition to offering insight into transient carrier trapping, gate leakage, and current collapse processes under realistic electrothermal settings, this simulation framework substantially resembles experimental bias sweeps.

Barrier Layer Trap Density the trap concentration (acceptor type) in the AlGaN barrier layer is studied by simulating the IV characteristics of the device for various trap densities.

Figure 5.14 shows the Drain current characteristics for three different trap densities (NT). An increase in trap density results in a decrease in the 2D electron gas concentration, which results in a decrease in the drain current of the device.

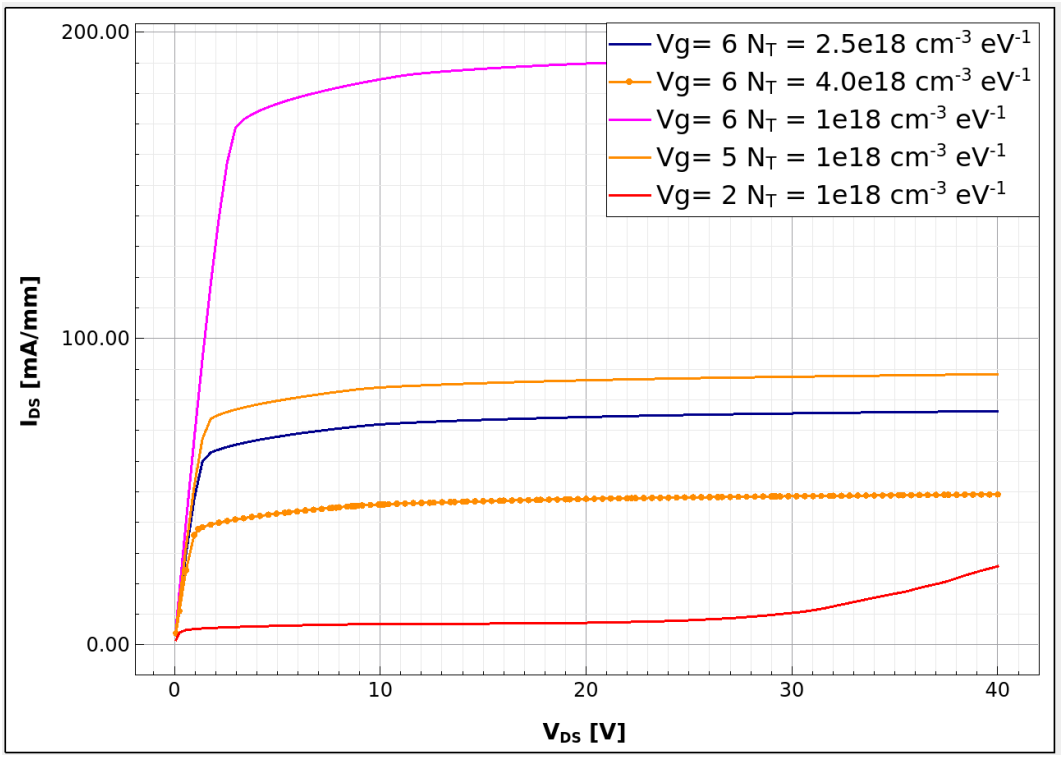


Figure 5.14 Drain Current characteristic at different Gate voltages and different Trap densities.

Analysis of Output Characteristics with Varying Trap Densities and Gate Voltages

Key Observations:

Effect of Trap Density (N_T): For a fixed gate voltage (Vg= 6V), increasing the trap density from 1×10^{18} to 4×10^{18} (compare magenta, blue, and orange curves) results in a significant reduction in the drain current. This indicates that higher trap densities in the device channel or barrier layer capture more carriers, thereby reducing the available free electrons for conduction and degrading device performance.

This analysis clearly shows that deep-level traps have a detrimental effect on the drain current, especially at higher densities, and that increasing the gate voltage can partially compensate for this effect by enhancing channel formation. Minimizing trap densities through optimized material growth and processing is therefore crucial for achieving high-performance and reliable p-GaN HEMTs

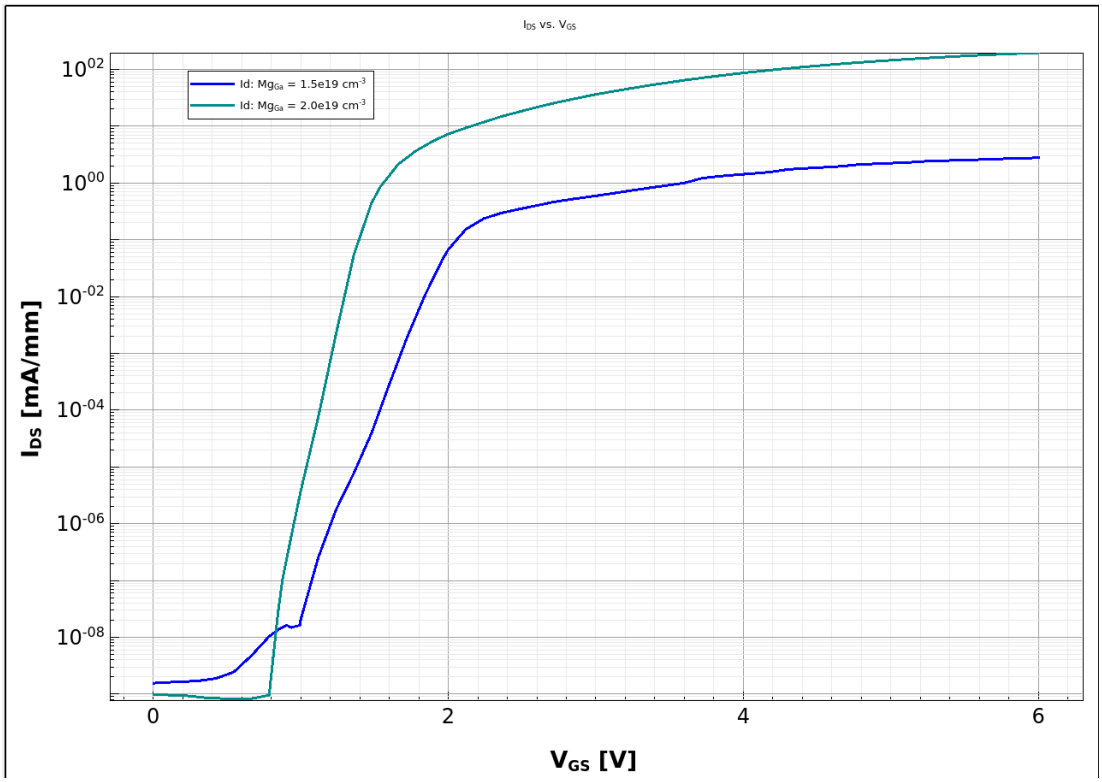


Figure 5.15 Drain Current characteristic at P-GaN doping

A time-dependent simulation was set up in two main stages to mimic experimental bias sweeps under transient conditions in order to derive the transfer characteristics (Id–Vg) of the AlGaN/GaN HEMT. In order to guarantee convergence of the electrostatic potential in the absence of free carriers, the simulation starts with a Poisson-only solution with a high iteration count and a low right-hand side (RHS) tolerance. A coupled Poisson–Electron–Hole solution is then used to achieve a steady and reliable electrothermal equilibrium. To give a reference profile at zero bias, a preliminary plot of the carrier distribution is taken at this starting state. Using adaptive time-stepping for both physical realism and numerical precision, the drain voltage is raised from 0 V to 40 V over a one-second period in the first transient step.

Before sweeping the gate, this process makes sure the channel is constructed. In order to see how the drain current changes as a function of gate bias, the gate voltage is progressively raised in the second phase from 0 V to its maximum value (6 V) during the course of the following simulated second. The dynamic behavior of carrier transport, including any transient effects associated to traps, is captured by coupled solutions to the continuity and Poisson equations throughout this sweep. At every gate step, the drain

current is measured and stored with spatially defined plots for later examination. With this technique, subthreshold behavior, threshold voltage, and transconductance properties can be accurately extracted, and trapping phenomena under gate modulation may be better understood.

In contrast, the gate leakage current characteristic is being plotted at three different trap densities (NT). Furthermore, figure 5.16 makes it very evident that gate leakage increases with density.

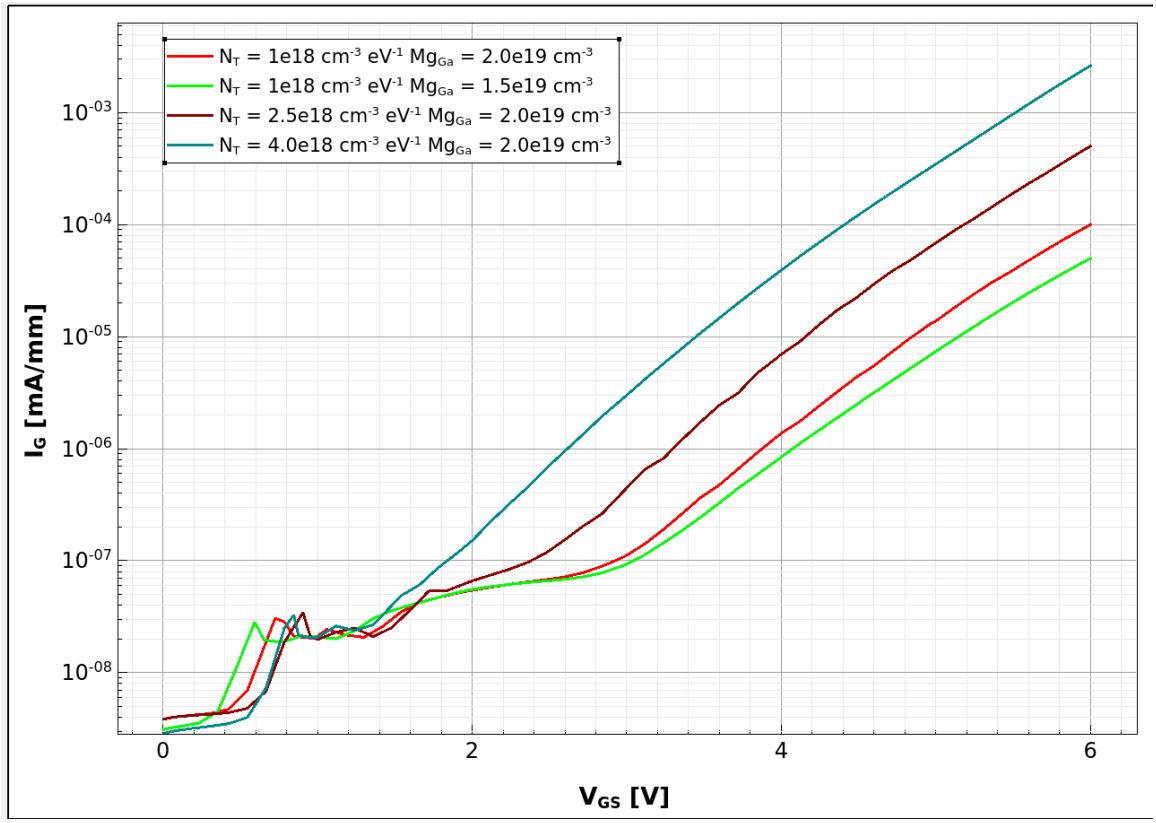


Figure 5.16 Gate Leakage Current characteristic at different doping concentrations of Magnesium and different Trap densities.

Analysis of Gate Leakage Current in p-GaN/AlGaN/GaN HEMTs with Variable Trap Densities

This comprehensive analysis examines the impact of AlGaN barrier layer trap states and p-GaN doping concentration on gate leakage current characteristics in p-GaN gate high electron mobility transistors (HEMTs). The simulation data reveals critical relationships between trap density, magnesium doping levels, and leakage current behavior across varying gate voltage conditions.

Trap Density Effects on Leakage Current Magnitude

The experimental data demonstrates a strong correlation between trap density (NT) in the AlGaN layer and gate leakage current magnitude. With magnesium doping concentration held constant at 2.0×10^{19} cm^{-3}, a systematic progression in leakage current appears as trap density increases. The device with NT = 4.0×10^{18} cm^{-3} eV^{-1} (teal curve) exhibits substantially higher leakage current—approximately 2×10^{-3} mA/mm at VGS = 6V compared to the baseline configuration with NT = 1.0×10^{18} cm^{-3} eV^{-1} (red curve), which shows leakage of approximately 1×10^{-4} mA/mm at the same voltage.

This relationship suggests trap states function as additional current pathways through the barrier layer. The exponential relationship between trap density and leakage current indicates that trap-assisted tunneling mechanisms become increasingly efficient as more trap states become available for carrier capture and emission. The intermediate case (NT = 2.5×10^{18} cm^{-3} eV^{-1}, brown curve) confirms this proportional relationship, exhibiting leakage levels between the two extremes.

Magnesium Doping Concentration Influence

An unexpected finding emerges when comparing devices with identical trap density (NT = 1.0×10^{18} cm^{-3} eV^{-1}) but different magnesium doping concentrations. The device with higher MgGa concentration (2.0×10^{19} cm^{-3}, red curve) exhibits consistently greater leakage current than its counterpart with lower MgGa concentration (1.5×10^{19} cm^{-3}, green curve). This difference becomes particularly pronounced at higher gate voltages, where at VGS = 6V, the leakage current differs by approximately a factor of two.

This observation contradicts conventional understanding that higher p-GaN doping improves leakage characteristics. The phenomenon might be explained through several mechanisms: increased doping may alter the electric field distribution at the p-GaN/AlGaN interface, potentially reducing effective barrier height; higher doping could enhance trap-assisted tunneling by modifying the energetic alignment between trap states and carrier bands; or the increased doping might introduce additional structural defects that facilitate leakage paths.

Voltage-Dependent Conduction Mechanisms

The data reveals distinct voltage-dependent behavior across all device configurations. Three characteristic regimes are evident:

1. Low-voltage regime (VGS < 1V): All configurations exhibit relatively stable, low leakage currents (3-4×10^{-8} mA/mm) with minimal dependence on trap density or doping concentration. This suggests that intrinsic leakage mechanisms dominate in this region, possibly related to thermionic emission over the barrier.
2. Transition regime (1V < VGS < 2.5V): Leakage currents begin to differentiate by configuration, with an irregular transition behavior suggesting competition between multiple conduction mechanisms. The non-monotonic variations in this region may indicate activation of different trap levels as the gate bias increases.
3. High-voltage regime (VGS > 2.5V): All configurations exhibit exponential current increase, but with significantly different rates. The steepest increase corresponds to the highest trap density (teal curve), suggesting that trap-assisted tunneling or Poole-Frenkel emission becomes the dominant mechanism, with efficiency proportional to trap concentration.

Conclusion

This analysis demonstrates that trap states within the AlGaN barrier layer fundamentally limit gate leakage performance in p-GaN HEMTs. Trap density emerges as the primary determinant of leakage current, with a non-linear relationship that becomes increasingly pronounced at higher gate voltages. The unexpected influence of p-GaN doping reveals complex interactions between design parameters that must be carefully balanced for optimal device performance.

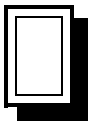
Future device engineering should focus on developing growth and processing techniques that minimize trap formation while implementing optimized doping profiles to achieve the desired threshold voltage with minimal leakage penalty. These findings provide a foundation for developing next-generation p-GaN gate HEMTs with improved leakage characteristics for high-efficiency power conversion applications.

5.6 Conclusion

This thesis presents a simulation-based investigation of deep-level traps in the barrier layer and at the AlGaN/GaN interface of GaN-based power HEMTs using Sentaurus TCAD. The traps were introduced to model the effects of electrothermal stress, which are known to impact device reliability and performance over time. The results show that an increase in trap concentration leads to a notable rise in gate leakage current, likely due to enhanced trap-assisted tunneling mechanisms. Simultaneously, the drain current decreases with higher trap densities, indicating carrier scattering and reduced channel conductivity. In the second part of the study, magnesium doping was introduced in the p-type gate region. It was found that as the Mg concentration increased, the gate leakage current significantly decreased, suggesting better gate control and suppression of leakage pathways. These results highlight the critical role of trap behavior and gate engineering in the overall performance and stability of GaN HEMTs, especially under high-stress power applications.

5.5 Future Scope

Building on the insights gained from this simulation study, several directions for future research are identified. One important extension would be to model the transient response of traps under pulsed or switching conditions, to better reflect the behavior of HEMTs in real-world applications such as power converters or RF amplifiers. Additionally, incorporating temperature-dependent trap models can enhance the understanding of thermal degradation mechanisms. Further exploration of the impact of trap spatial distribution, energy level, and capture cross-section would also be valuable. On the materials front, optimizing Mg doping profiles and examining other potential dopants could lead to improved gate performance and reduced leakage. Finally, integrating this electrothermal degradation modeling into a full device reliability simulation framework can help predict long-term failure mechanisms and guide the design of more robust and efficient GaN-based power devices.



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